

FORM PTO-1390
(REV 10-94)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER

TRANSMITTAL LETTER TO THE UNITED STATES
DESIGNATED/ELECTED OFFICE (DO/EO/US)
CONCERNING A FILING UNDER 35 U.S.C. 371

30019.70USWO

U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5)

Unknown

09/762720

INTERNATIONAL APPLICATION NO.

PCT/US99/20792

INTERNATIONAL FILING DATE

September 10, 1999

PRIORITY DATE CLAIMED

September 10, 1998

TITLE OF INVENTION

A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

APPLICANT(S) FOR DO/EO/US

MACNALLY et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(I).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
 - a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
 - b. ☒ has been transmitted by the International Bureau.
 - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
 - a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
 - b. ☐ have been transmitted by the International Bureau.
 - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
 - d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An unsigned oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment and attached Abstract.
☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information: International Preliminary Examination Report and annexes; courtesy copy of PCT/US99/20792 publication page and application; 16 sheets of formal drawings; Demand; Information Concerning elected Offices Notified of their Election; Notification of Receipt of Demand; International Search Report; Notification Concerning Submission or Transmittal of Priority Document; Notice Informing the Applicant of the Communication of the Application to the Designated Offices; Request

U.S. APPLICATION NO (If known, see 37 C.F.R. 1.5)

INTERNATIONAL APPLICATION NO

ATTORNEY'S DOCKET NUMBER

Unknown

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PCT/US99/20792

30019.70USWO

17. *☒ The following fees are submitted:**BASIC NATIONAL FEE (37 CFR 1.492(a) (1)-(5)):**

Search Report has been prepared by the EPO or JPO.....\$860.00

International preliminary examination fee paid to USPTO

(37 CFR 1.492(a)(1)).....\$690.00

No international preliminary examination fee paid to USPTO (37 CFR 1.482)

but international search fee paid to USPTO (37 CFR 1.445(a)(2)).....\$710.00

Neither international preliminary examination fee (37 CFR 1.482) nor

international search fee (37 CFR 1.445(a)(3)) paid to USPTO \$1000.00

International preliminary examination fee paid to USPTO (37 CFR 1.482)

and all claims satisfied provisions of PCT Article 33(2)-(4)\$100.00

ENTER APPROPRIATE BASIC FEE AMOUNT = \$860.00Surcharge of **\$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30
months from the earliest claimed priority date (37 CFR 1.492(e)).

\$0

CLAIMS

NUMBER FILED

NUMBER EXTRA

RATE

Total claims

6

-20 = 0

X \$18.00

\$0

Independent claims

2

-3 = 0

X \$80.00

\$0

MULTIPLE DEPENDENT CLAIM(S) (if applicable)

+ \$260.00

\$0

TOTAL OF ABOVE CALCULATIONS = \$860.00Reduction by 1/2 for filing by small entity, if applicable. Small entity status is claimed
pursuant to 37 CFR 1.27

\$0

SUBTOTAL = \$860.00Processing fee of **\$130.00** for furnishing the English translation later than ☐ 20 ☐ 30
months from the earliest claimed priority date (37 CFR 1.492(f)).

+ \$0

TOTAL NATIONAL FEE = \$860.00Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be
accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property

+ \$0

TOTAL FEES ENCLOSED = \$860.00Amount to be:
refunded \$

charged \$

a. ☒ Check(s) in the amount of \$860.00 to cover the above fees is enclosed.b. ☐ Please charge my Deposit Account No. _____ in the amount of \$ _____ to cover the above fees.
A duplicate copy of this sheet is enclosed.c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any
overpayment to Deposit Account No. 13-2725.**NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR
1.137(a) or (b)) must be filed and granted to restore the application to pending status.**

SEND ALL CORRESPONDENCE TO

Min (Amy) S. Xu

MERCHANT & GOULD

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Minneapolis, MN 55402-0903

SIGNATURE: 

NAME: Min (Amy) S. Xu

REGISTRATION NUMBER: 39,536

Applicant: MACNALLY et al.
 Docket: 30019.70USWO
 Title: A SINGLE-CHIMP CMOS DIRECT-CONVERSION TRANSCEIVER

CERTIFICATE UNDER 37 CFR 1.10

'Express Mail' mailing label number: EL658339920US

Date of Deposit: February 8, 2001

I hereby certify that this paper or fee is being deposited with the United States Postal Service 'Express Mail Post Office To Addressee' service under 37 CFR 1.10 and is addressed to the Assistant Commissioner for Patents, Washington, D C 20231.

By: 
 Name: Brian Maharaj

BOX PCT
 Assistant Commissioner for Patents
 Washington, D.C. 20231

Sir:

We are transmitting herewith the attached:


- ☒ Transmittal sheet, in duplicate, containing Certificate under 37 CFR 1.10.
- ☒ National Stage PCT Patent Application: Spec. 16 pgs; 6 claims
 The fee has been calculated as shown below in the 'Claims as Filed' table.
- ☒ 16 sheets of formal drawings
- ☒ An unsigned Combined Declaration and Power of Attorney
- ☒ A check in the amount of \$860.00 to cover the Filing Fee
- ☒ Other: Preliminary Amendment and attached Abstract; courtesy copy of PCT/US99/20792 publication page; International Preliminary Examination Report and annexes; Information Concerning Elected Offices Notified of their Election; Notification of Receipt of Demand; Demand; International Search Report; Notification Concerning Submission of Transmittal of Priority Document; Notice Informing the Applicant of the Communication of the International Application to the Designated Offices; Request
- ☒ Return postcard

CLAIMS AS FILED

Number of Claims Filed		In Excess of:		Number Extra		Rate		Fee
Basic Filing Fee								\$860.00
Total Claims								
6	-	20	=	0	x	0.00	=	\$0.00
Independent Claims								
2	-	3	=	0	x	0.00	=	\$0.00
MULTIPLE DEPENDENT CLAIM FEE								\$0.00
TOTAL FILING FEE								\$860.00

Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725. A duplicate of this sheet is enclosed.

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By: 
 Name: Min (Amy) S. Xu
 Reg. No.: 39,536
 Initials: MSX:IPD:jjw

09/762720

JC02 Rec'd PCT/PTO 08 FEB 2001
PATENT

S/N Unknown

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	MACNALLY et al.	Serial No.:	Unknown
Filing Date:	Concurrent herewith	Attorney Docket:	30019.70USWO
International Application No.:	PCT/US99/20792	International Filing Date:	September 10, 1999
Title:	A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER		

CERTIFICATE UNDER 37 CFR 1.10

'Express Mail' mailing label number: EL658339920US

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I hereby certify that this paper or fee is being deposited with the United States Postal Service 'Express Mail Post Office To Addressee' service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner of Patents and Trademarks, Washington, D.C. 20231.

By: 
Name: Brian MaharajPRELIMINARY AMENDMENT

Box PCT

Assistant Commissioner for Patents
Washington, D. C. 20231

Dear Sir:

In connection with the above-identified application filed herewith, please enter the following preliminary amendment, which is based on claims amended in prosecution of the international application and published in the International Preliminary Examination Report, a copy of which is enclosed herewith:

IN THE ABSTRACT

Insert the attached Abstract page into the application as the last page thereof.

IN THE SPECIFICATION

A courtesy copy of the present specification is enclosed herewith. However, the World Intellectual Property Office (WIPO) copy should be relied upon if it is already in the U.S. Patent Office.

REMARKS

A new abstract page is supplied to conform to that appearing on the publication page of the WIPO application, but the new Abstract is typed on a separate page as required by U.S. practice.

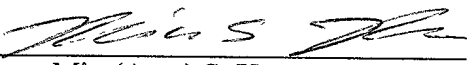
Applicants respectfully request that the preliminary amendment described herein be entered into the record prior to calculation of the filing fee and prior to examination and consideration of the above-identified application.

If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicants' primary attorney-of record, Min (Amy) S. Xu (Reg. No. 39,536), at (612) 336-4733.

Respectfully submitted,

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Dated: February 8, 2001

By 
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MSX:IPD:jjw

ABSTRACT

A single-chip CMOS direct conversion transceiver includes an RF circuit, a transmitter having a synthesizer, a receiver having a baseband filter, and a demodulator.

- 5 The synthesizer is coupled to the RF circuit. The baseband filter is coupled to the RF circuit and the synthesizer. The demodulator is coupled to the baseband filter. The RF circuit, the synthesizer, the baseband filter, and the demodulator are arranged and configured in CMOS devices and provide a complete interface between an antenna and a voiceband codec.

A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

BACKGROUND OF THE INVENTION1. Field of the Invention.

5 This invention relates in general to communication systems, and more particularly to a single-chip CMOS direct-conversion transceiver.

2. Description of Related Art.

Today's wireless communications markets are being driven by a multitude of user benefits. Products such as cellular phones, cordless phones, pagers, and the like
10 have freed corporate and individual users from their desks and homes and are driving the demand for additional equipment and systems to increase their utility. As a result digital radio personal communications devices will play an increasingly important role in the overall communications infrastructure in the next decade.

Mixed-signal integration and power management have taken on added
15 importance now that analog and mixed analog-digital ICs have become the fastest-growing segment of the semiconductor industry. Integration strategies for multimedia consoles, cellular telephones and battery-powered portables are being developed, as well as applications for less integrated but highly specialized building blocks that serve multiple markets. These building blocks include data converters,
20 amplifiers and voltage regulators. Makers of amplifiers and regulators often eschew integration in CMOS, but strive for compact size and reduced costs with microminiature packaging.

One important aspect of digital radio personal communications devices is the integration of the RF sections of transceivers. Compared to other types of integrated

circuits, the level of integration in the RF sections of transceivers is still relatively low. Considerations of power dissipation, form factor, and cost dictate that the RF/IF portions of these devices evolve to higher levels of integration than is true at present. Nevertheless, there are some key barriers to realizing these higher levels of
5 integration.

A high level of integration is critical in lowering the cost of electronics for communication systems such as cellular phones, cordless phones, and wireless LANs. Increasing levels of transceiver integration are being reported, e.g., RF, baseband analog, and mixed-signal circuits have been integrated. Further, RF,
10 baseband analog, and voltage-controlled oscillator (VCO) circuits have also been realized in a single die.

It can be seen that there is a need for a fully-integrated transceiver.

It also can be seen that there is a need for a fully-integrated transceiver that incorporates RF circuits, synthesizer, baseband filters, demodulator, and extensive
15 digital control functions.

SUMMARY OF THE INVENTION

To overcome the limitations in the prior art described above, and to overcome other limitations that will become apparent upon reading and understanding the present specification, the present invention discloses a single-chip
20 CMOS direct-conversion transceiver.

In one embodiment of the present invention, the single-chip CMOS direct-conversion transceiver includes an RF circuit, a transmitter having a synthesizer, a receiver having a baseband filter, and a demodulator. The synthesizer is coupled to the RF circuit. The baseband filter is coupled to the RF circuit and the synthesizer.
25 The demodulator is coupled to the baseband filter. The RF circuit, the synthesizer,

the baseband filter, and the demodulator are arranged and configured in CMOS devices and provide a complete interface between an antenna and a voiceband codec.

Another aspect of the invention is that the transceiver further includes a time-division duplex (TDD) circuit for ensuring isolating between the transmitter
5 and the receiver.

A further aspect of the invention is that the transmitter and the receiver share the same RF port which interfaces with an external antenna.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent
10 corresponding parts throughout:

Fig. 1 illustrates a block diagram of the single-chip CMOS transceiver according to the present invention;

Fig. 2 illustrates the low noise amplifier according to the present invention;

Fig. 3 is a circuit diagram of the mixer and antialias filter according to the
15 present invention;

Fig. 4 illustrates a plot of the receiver bit error rate (BER);

Fig. 5 is a table illustrating the performance characteristics of the single-chip CMOS transceiver;

Fig. 6 illustrates the transmit spectrum for 20 dBm output power;

20 Fig. 7 illustrates the voltage controlled oscillator;

Fig. 8 illustrates a block diagram of the synthesizer;

Fig. 9 is a phase noise plot for the single-chip CMOS transceiver;

Fig. 10 is a plot of the unmodulated output spectrum for the single-chip CMOS transceiver;

25 Fig. 11 illustrates the measured I/Q constellation for a -80dBm RF input;

Fig. 12 illustrates a circuit diagram for the power amplifier;

Fig. 13 illustrates the die micrograph of the single-chip CMOS transceiver;

Fig. 14 is the intermodulation (IM) plot for the entire receive path;

Fig. 15 shows the measured step response of the channel filters; and

Fig. 16 shows a change in the output levels of the channel filters in response

5 to a change in the amplitude of a receive burst.

DETAILED DESCRIPTION OF THE INVENTION

In the following description of the exemplary embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration the specific embodiment in which the invention may be practiced.

10 It is to be understood that other embodiments may be utilized as structural changes may be made without departing from the scope of the present invention.

In an embodiment of the present invention is a specific combination of building blocks that realize a monolithic transceiver for digital communication that may be used for various media.

15 A function of the monolithic transceiver is to convert digital data to an analog signal suitable for transmission and to convert a received analog signal into digital data. In practice, there will be a finite bit error rate in the transmission, propagation and reception processes. The specific BER that is tolerable depends on the application. In some cases, the input to one monolithic transceiver and at the
20 output of another monolithic transceiver may be different because of intentional signal processing.

Typically, a pair of monolithic transceivers is used for full duplex communication. However, more than two monolithic transceivers can be used in more complex communication systems. In some cases, the communication is only
25 required from one point to another without full duplex. In some cases, different media may be used for each direction of a full duplex system. In some cases, the

monolithic transceiver may include multiple receivers and transmitters. In some cases, the analog signal may be converted from one media to another along propagation. Each receiver and transmitter in the monolithic transceiver may be intended for different media.

5 The digital data communicated may originate from an arbitrary source and will be delivered to an arbitrary target. Common sources and targets include: (1) Computers, (2) Sensors, (3) Magnetic or optical media, (4) Other monolithic transceivers.

10 The analog signal is typically propagated using one or more of the following methods: (5) Free space radiation, (6) Transmission lines: (a) Coaxial cables, (b) Twisted pairs, (c) Waveguides, (7) Fiber optics, (8) Sonar in liquid, solid or gas media.

15 The elements used in the monolithic transceiver include the following means: (9) Digital processing and control circuits, (10) Analog-to-Digital, Analog, Digital-to-Analog processing circuits, (11) Media interface processing circuits.

20 The digital processing circuits are used to condition data from a source into internal digital data in the monolithic transceiver destined for transmission and to condition received internal digital data in the monolithic transceiver for a target. The digital control circuits are used to coordinate the activities of the monolithic transceiver necessary to accomplish half-duplex, full-duplex or more complex communication systems and to coordinate digital communication with the source and target.

25 The analog-to-digital, analog and digital-to-analog processing provides the interface between the digital and analog domains. These functions are commonly accomplished using analog circuits such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), filters and automatic gain control systems. In

some cases, these functions may be part of or inherent to other analog functions such as a demodulator.

The media interface processing circuits provide the interface between the analog domain used for transmission and the analog domain used in the monolithic transceiver. In a RF monolithic transceiver, these interface circuits include a low noise amplifier (LNA), power amplifier (PA), mixer and synthesizer. Each type of media has its own specific interface circuit appropriate for that media.

More specifically, the monolithic transceiver design includes the following choices: (12) Time division duplex (TD) or frequency division duplex (FDD), (13) Modulation technique, (14) Narrow-band or wide-band communication, (15) Direct-sequence or frequency hopping spreading and despreading, (16) Silicon or heterojunction semiconductor platforms, (17) MOS or bipolar devices.

The specific attributes chosen may ease implementation of the monolithic transceiver that may make the monolithic transceiver particularly attractive for certain markets.

More specifically, the use of silicon MOS technologies permits the monolithic transceiver to take an advantage of attributes of MOS devices in general and to take an advantage of attributes of short-channel MOS devices in modern CMOS technologies for particular wireless applications.

The use of MOS devices permits the digital processing and control circuits to be accomplished with high density and lower power. This is important because of well-known attributes of MOS devices for logic implementation. This permits implementation of sophisticated digital signal processing for portable wireless applications, as an example.

The use of MOS devices permits analog, A/D, D/A processing circuits to be accomplished using switched-capacitor techniques. This is important because, in

general, MOS devices have the attribute of an extremely large on-state to off-state conductance ratio necessary for an excellent switch. This switch is the basis for sampled-charge based approaches. The use of MOS devices permit a rich and sophisticated array of sampled-data systems to be implemented including ADCs, DACs and filters.

The use of MOS devices permits media interface processing circuits to be accomplished using amplifiers, mixers, and frequency synthesizers. In particular, recent advances in short-channel MOS devices permit the media interface processing circuits to be accomplished at microwave frequencies used in many wireless applications.

More specifically, the use of Bipolar or BiCMOS technology may be used to implement the monolithic transceiver.

The use of BiCMOS technology can be used to accomplish a monolithic transceiver with the digital processing and control circuits using CMOS devices, the analog, A/D, D/A circuits and the media interface processing circuits using a combination of bipolar or CMOS devices.

The use of bipolar technology can be used to accomplish the monolithic transceiver. This approach may be better for specialized applications such as millimeter wave systems where HBT devices are more appropriate. Other applications where bipolar devices may be a better choice include fiber-optic applications.

The use of bipolar devices does not permit the digital processing and control circuits to be accomplished with high density or low power. However, high speed may be the advantage.

The use of bipolar devices does not permit the analog, A/D, D/A circuits to use switched-capacitor techniques. This is a major limitation because of

sophistication possible with switched-capacitor sampled-data systems. The bipolar device can be used to implement sampled-data systems using other techniques such as switched-current approaches. However, sampled-data systems built with these approaches are far less flexible and use far more power than switched-capacitor techniques.

The use of bipolar devices does permit the media interface processing circuits to be accomplished with more ease at present. However, future advances in CMOS process technology may favor CMOS devices for the media interface processing circuits.

More specifically, the choice of modulation technique influences the complexity of certain blocks. For example, the use of FSK modulation relaxes the linearity requirement of the PA. This is important as at present, CMOS PAs are not easily accomplished with high linearity.

The following description discusses one embodiment of a monolithic transceiver implementation that uses CMOS technology, FSK modulation, switched-capacitor techniques for sampled-data systems and a relatively complex digital signal processor and control unit.

In one embodiment, the present invention provides a single-chip CMOS direct-conversion transceiver. As stated above, a high level of integration is critical in lowering the cost of electronics for communication systems such as cellular phones, cordless phones, and wireless LANs. The present invention provides a fully-integrated transceiver 100, shown in Fig. 1, that incorporates RF circuits 102, 104, synthesizer 106, baseband filters 108, demodulator 110, and digital signal processing. The few off-chip components include an ISM band filter 112, a balun 114, an RF matching network 116, an RC loop filter for the PLL 118, a crystal resonator 120, and a resistor 122 for biasing. The use of a transmit/receive (T/R)

switch is avoided by sharing a single RF port between a transmitter 124 and a receiver 126. An offset cancellation method attenuates offsets in the baseband without sacrificing bandwidth in the direct conversion receiver 126. Careful circuit, timing, and layout considerations provide isolation between the sensitive RF signal and the digital switching noise. The IC has been fabricated in 0.6- μ m CMOS and provides a complete interface between an antenna 128 and a voiceband codec 130.

Architectural and circuit techniques have made it possible to achieve this level of integration without sacrificing performance. Time-division duplex (TDD) ensures isolation between the transmitter 124 and the receiver 126. Direct conversion makes it possible to eliminate expensive, off-chip radio frequency (RF) image reject filters and diplexer, and to replace off-chip intermediate frequency (IF) channel select filters with on-chip low pass filters.

Active on-chip offset reduction by means of feedback and feedforward loops has been combined with a digitally controlled automatic gain control (AGC) circuit 132 that settles within the 160- μ s preamble of the receive burst.

In a direct conversion receiver 126, static and varying DC offsets within the base band I and Q channel amplifiers and filters limit the architecture's usefulness. In the past, AC coupling or high pass filtering has been used to remove the DC offset from the signal. However, this removes some of the useful DC or near DC energy from the signal causing degradation to the signal. The present invention uses a combined feedback and feedforward offset cancellation technique with DC signal response to cancel the DC offset problem while at the same time providing for a DC response to the base band signals of interest.

The main feature of the feed forward offset cancellation architecture is its capability to cancel low frequency (DC to 5 kHz) offsets caused by LO leakage and other non-ideal component induced offsets while at the same time maintaining a DC

response to the signal. This is accomplished by two main components of the architecture.

The first main component is the signal format. A signal format was chosen such that the I and Q base band signals exhibit a positive and negative peak within a certain time frame, 6.66 micro-seconds was chosen. The peaks and valleys of the I and Q signals from one time frame to the next are required to be approximately equal.

The second main component is a positive and negative peak detector which determines the peaks and valleys of the signal over a certain time frame (6.66uS).

The offset is then the addition of the positive and negative peaks divided by two.

A fully-differential analog signal path minimizes supply and substrate noise coupling. To further reduce coupling, transitions of digital signals have been minimized near the sampling edge of baseband switched-capacitor circuits.

Source-coupled logic has been utilized in the PLL frequency dividers to reduce substrate noise injection, while CMOS logic gates have been used in a burst-mode controller (BMC) 134 to achieve low power dissipation and high circuit density. An automatic calibration technique has allowed the integration of a 1.8-GHz LC VCO with a wide tuning range. The receiver 126 has a maximum gain of 106 dB and a sensitivity of -104 dBm.

A low noise amplifier (LNA) 138 and the power amplifier (PA) 104 designs make it possible to share a common RF port 140, thereby eliminating the need for an external transmitter/receiver switch. The transmitter 124 and receiver 126 are attached to the filter/antenna port of a radio transceiver without the need for a costly antenna switch in a time division duplex system.

Radio transceivers usually require both a Low Noise Amplifier or (LNA) for clear reception and a Power Amplifier or (PA) for transmitting over long distances.

In a time division duplex or (TDD) transceiver 100, the transmitter 124 and receiver 126 are not utilized simultaneously. When the transmitter 124 is on, the receiver 126 is off, and when the receiver 126 is on, the transmitter 124 is off. For a typical TDD transceiver 100, the receive LNA 138 is powered down during the transmit cycle to conserve power, and the transmit power amplifier 140 is powered down while the receiver 126 is on.

In the past, the LNAs and PAs have been designed utilizing bipolar transistor technology. The bipolar LNAs and PA's are capable of powering down, however their respective input and output impedance while in the powered down state do not allow them to be connected together in a TDD system. The powered down LNA will attenuate the output power of the PA and may even be damaged by the PA. The powered down PA will lower the impedance that the LNA "sees" and will attenuate the incoming signal from the antenna.

To get around the varying impedance problem, LNA and PA typically use their own set of different matching components to produce a 50 Ohm LNA input impedance and 50 Ohm PA output impedance. This topology is then combined with an antenna switch so that the off state impedances of either the LNA or the PA will not harm the 50 match achieved by the different matching components. However, the antenna switch can be costly, and the transmit and receive signals are still attenuated somewhat by the switch itself. In addition a control circuit must be used to switch the antenna switch.

According to the present invention, the antenna interface requires only one RF combined input/output port thereby reducing IC package pin count and the number of external components. An impedance transformation network of 25 to 50 ohm network is used to ease the LNA requirement. A singly matched network is used for PA since putting required matching 50 ohm will limit the theoretical power

efficiency to less than 50% and will degrade the power efficiency achieved in practice.

The LNA 138, shown in Fig. 2, is implemented as a cascade of two stages. The first stage employs a capacitively cross-coupled input pair, M1 and M2, that provides both gain and impedance matching in parallel with a differential pair, M3 and M4, for additional gain. The second stage of the LNA 138 is also a differential pair. All gain stages are loaded by on-chip spiral inductors. The combined LNA gain can be set to 12 dB or 28 dB.

The PA 140 is implemented as a three-stage, class AB amplifier. The first stage is a resistively loaded differential pair, the second stage is a common-source stage loaded with on-chip spiral inductors, and the output stage consists of large open drain devices whose drains are connected to the LNA input. The bias currents of the final stage are provided by off-chip RF chokes. The output power, measured at the balun, can be varied from +2 dBm to +20 dBm. Refer to Fig. 12.

A diagram of a mixer 142 and antialias filter 144 is shown in Fig. 3. The mixer's conversion gain is 14.3 dB. The mixer uses a double balanced structure without a tail current source to increase headroom. Biasing for the RF input transistors is performed by a replica circuit that suppresses transconductance variations with process and temperature. The LO input transistors operate as switches that steer a process and temperature independent current. The output of the mixer 142 is fed to a four-pole Butterworth antialias filter 144 with a cut-off frequency of 2.4 MHz.

Two biquad stages form the four-pole Butterworth antialias filter 144 with a nominal gain of 15.6 dB and a cut-off frequency of 2.4 MHz. Switched-capacitor I and Q baseband filters sample the output of the antialias filter 144 at 24 MHz, attenuate adjacent channels, and provide AGC 132. Each baseband signal path

comprises a fourth-order low pass Chebyshev filter, implemented with two biquad sections, followed by a group delay equalizer (GDE). The biquads and the GDE have a programmable gain of one or four. The filter is followed by a switched-capacitor variable gain amplifier (VGA) that is programmable with a gain of one, two, or four. This arrangement provides a baseband gain of 0 dB to 48 dB in 6 dB steps.

In a direct conversion receiver 126, LO leakage can lead to large offsets at the inputs to the baseband filters 108. Moreover, offsets in the switched-capacitor filter sections can accumulate and render the output signal undetectable. To overcome this problem, feedback integrators cancel offsets in the first biquad and in the GDE, as shown in Fig. 1. To prevent baseline wander from causing errors, the integrators are placed in a hold mode when data is transferred.

Switched-capacitor peak detector circuits 146 sample the maximum and minimum values of the filtered I and Q signals. The AGC controller 132 uses the peak detector 146 outputs to estimate the signal levels and adjusts the baseband gain accordingly. The outputs of the peak detectors 146 are also low pass filtered to estimate the residual offset in the outputs of the channel filters. The offset is then subtracted from the baseband filter output, and the resulting I and Q signals are fed to the BFSK demodulator 110.

The BFSK demodulator 110 is implemented with switched-capacitor circuits clocked at 6 MHz. It generates a digital output based on the direction of rotation of the I/Q constellation. The digital output of the demodulator 110 is processed by the on-chip BMC 134, comprising over 8000 CMOS standard cell gates, that performs clock recovery and direct sequence spreading and despreading. The receiver bit error rate (BER), shown in Fig. 4, illustrates the receiver sensitivity. Selectivity and blocking performance are given in the table in Fig. 5.

The single frequency synthesizer 106 creates both LO and PA input signals for receive and transmit, respectively. The circuit generates channels from 900 MHz to 930 MHz in 750kHz increments. During receiving, a divide-by-two circuit creates I and Q LO signals from the output of a VCO operating at twice the desired frequency in a high bandwidth PLL. During transmit, the PLL bandwidth is reduced allowing filtered transmit data to directly modulate the VCO while maintaining a constant center frequency. The transmit spectrum for 20 dBm output power is shown in Fig. 6. The VCO, shown in Fig. 7, is designed as a cross-coupled differential pair loaded by spiral inductors and by capacitors. The load capacitors include ac-coupled channel varactors, modulation varactors, and a bank of capacitors for automatic coarse frequency adjustment.

The synthesizer 106 architecture is shown in Fig. 8. The varactors are on chip. The VCO 148 operates at twice the carrier frequency in order to alleviate problems arising from PA pulling. Furthermore, it allows the robust creation of I and Q signals using a simple divide-by-two circuit. A phase noise plot is provided in Fig. 9, and the output spectrum is shown in Fig. 10.

The VCO 148 is automatically calibrated in a closed loop with control circuitry that digitally adjusts the capacitive load of the tank. The measured I/Q constellation for a -80dBm RF input is shown in Fig. 11. The PA circuit 140 is illustrated in Fig. 12. The power efficiency of the PA 140 is 20% at +20 dBm.

The measured performance, summarized in the table of Fig. 5, demonstrates that a single-chip CMOS transceiver 100 can successfully integrate the RF front end along with baseband analog circuits and a significant amount of standard cell digital circuits. Fig. 13 illustrates the die micrograph of the single-chip CMOS transceiver 100.

The intermodulation (IM) plot for the entire receive path is shown in Fig. 14.

This plot was generated by applying two tones that are 6 channels away from the carrier and recording the power of the IM product at the output of the baseband filters. The tones were chosen such that the IM products are well within the bandwidth of the baseband filters 108. The measurements include the influence of on-chip test buffers on the receiver linearity. The input signal power was measured at the input to the chip, and the LNA gain was in its "high" settings. The 1-dB compression point is limited by the switched-capacitor circuits and occurs at approximately 5V differential amplitude.

All switched-capacitor stages in the baseband filters 108, peak detectors 146, and demodulator 110 employ correlated double sampling (CDS) to attenuate their offsets and $1/f$ noise. To minimize offsets due to mismatch in sampling switches, NMOS rather than CMOS switches have been used. The four clock signals include two-phase, non-overlapping and delayed phases that are driven by voltage doublers. Static charge pumps drive the gain selection switches in the baseband filters 108 and VGA. Fig. 15 shows the measured step response of the channel filters. Fig. 16 shows a change in the output levels of the channel filters in response to a change in the amplitude of a receive burst.

The selectivity, as shown in the table of Fig. 5, was measured by applying a -83 dBm desired signal, then increasing the power of an interferer until the BER reached 10^{-3} . The difference between the power of the interferer and -83 dBm is the selectivity. This test was performed with the interferer within the desired channel as well as 1.5 MHz, 3 MHz, and 4.5 MHz from the carrier. When the interfering tone is 4.5 MHz from the carrier, the receiver's BER is limited by the linearity of the front end. Hence, this measurement represents the blocking performance of the receiver.

The foregoing description of the exemplary embodiment of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching.

What is claimed is:

1. A single-chip direct conversion transceiver, comprising:
an RF circuit;
a transmitter having a synthesizer;
5 a receiver having a baseband filter and a demodulator; and
wherein the synthesizer is coupled to the RF circuit, the baseband filter is coupled to the RF circuit, and the demodulator is coupled to the baseband filter.
- 10 2. The transceiver of claim 1, further comprising a time-division duplex (TDD) circuit for ensuring isolating between the transmitter and the receiver.
3. The transceiver of claim 1, wherein the transmitter and the receiver share the same RF port which interfaces with an external antenna.
- 15 4. The transceiver of claim 1, wherein the synthesizer performs FSK modulation.
5. A single-chip direct conversion receiver, comprising:
20 an RF circuit;
a baseband filter and a demodulator; and
wherein the baseband filter is coupled to the RF circuit, and the demodulator is coupled to the baseband filter.
- 25 6. The receiver of claim 5, wherein the demodulator performs FSK modulation.



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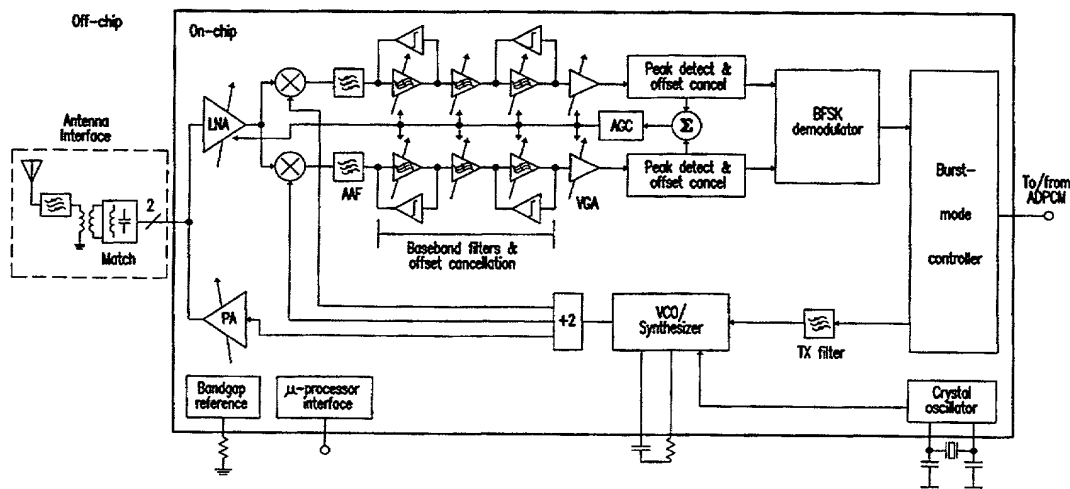
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(57) Abstract

A single-chip CMOS direct conversion transceiver includes an RF circuit, a transmitter having a synthesizer, a receiver having a baseband filter, and a demodulator. The synthesizer is coupled to the RF circuit. The baseband filter is coupled to the RF circuit and the synthesizer. The demodulator is coupled to the baseband filter. The RF circuit, the synthesizer, the baseband filter, and the demodulator are arranged and configured in CMOS devices and provide a complete interface between an antenna and a voiceband codec.

FIG. 1

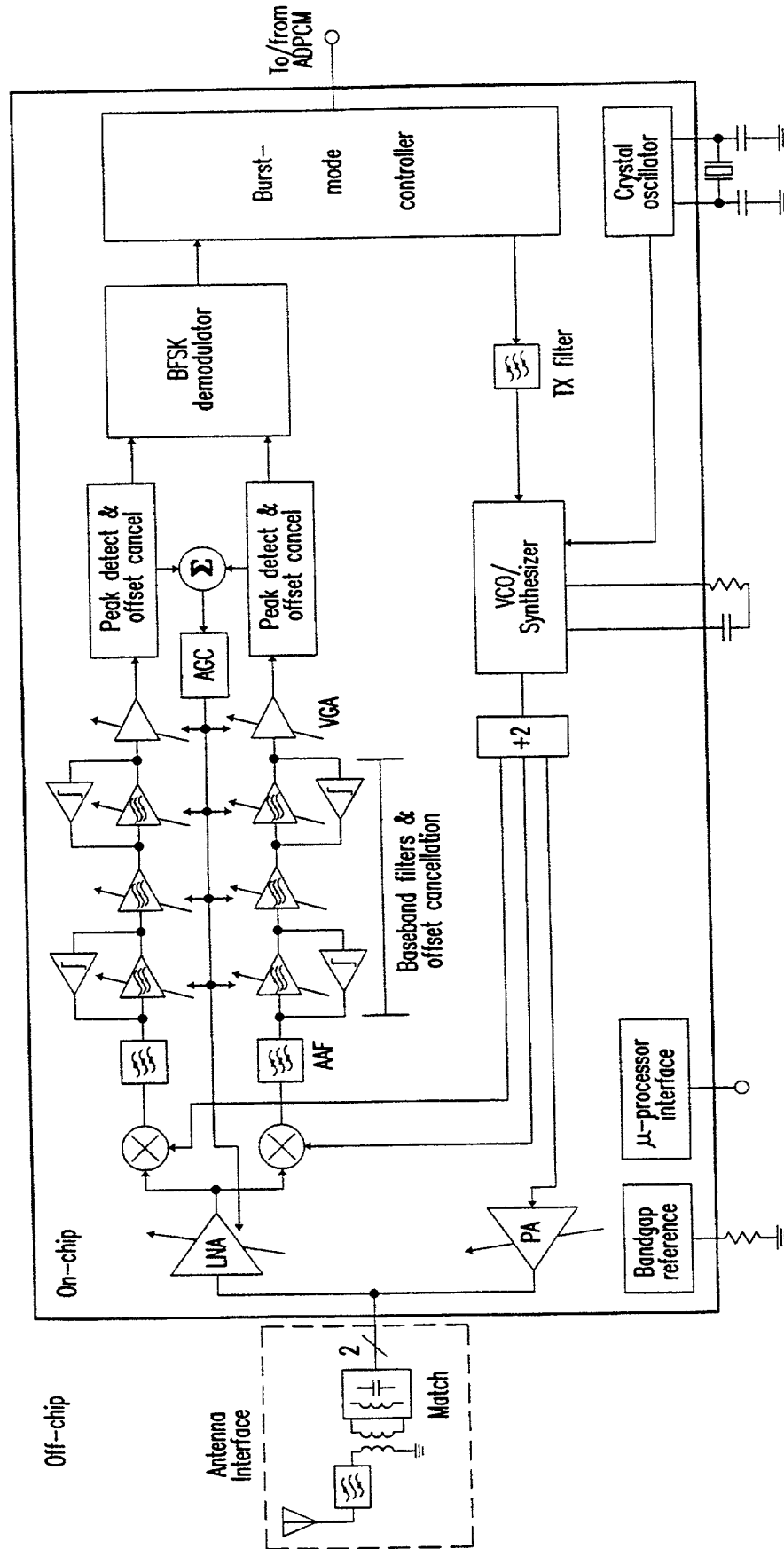
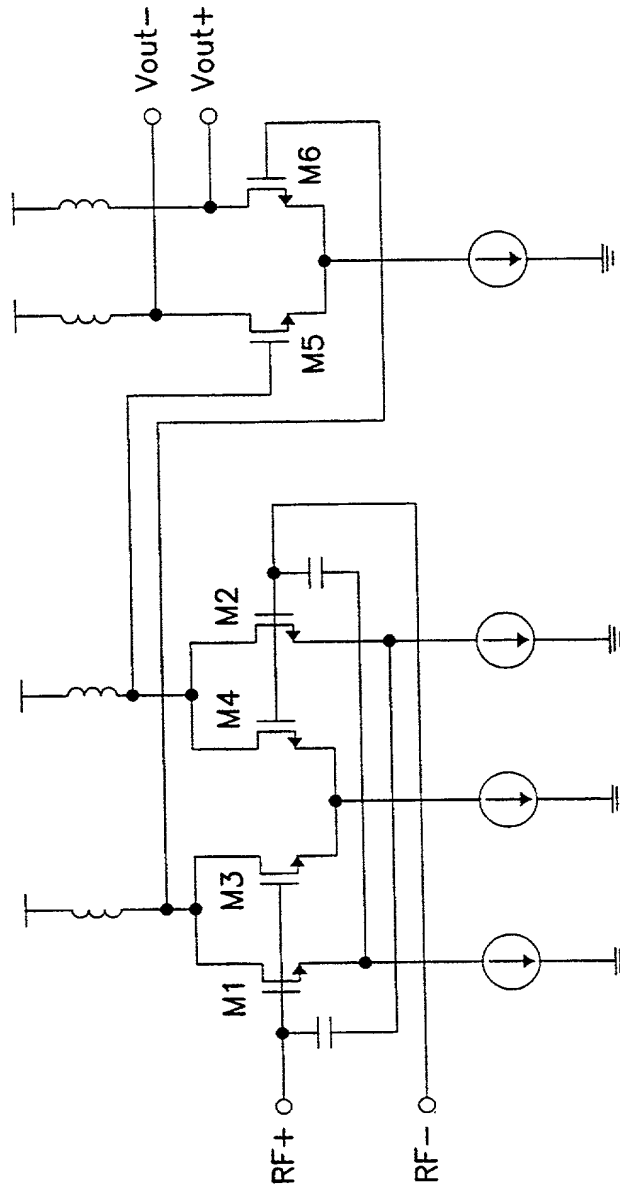


FIG. 2

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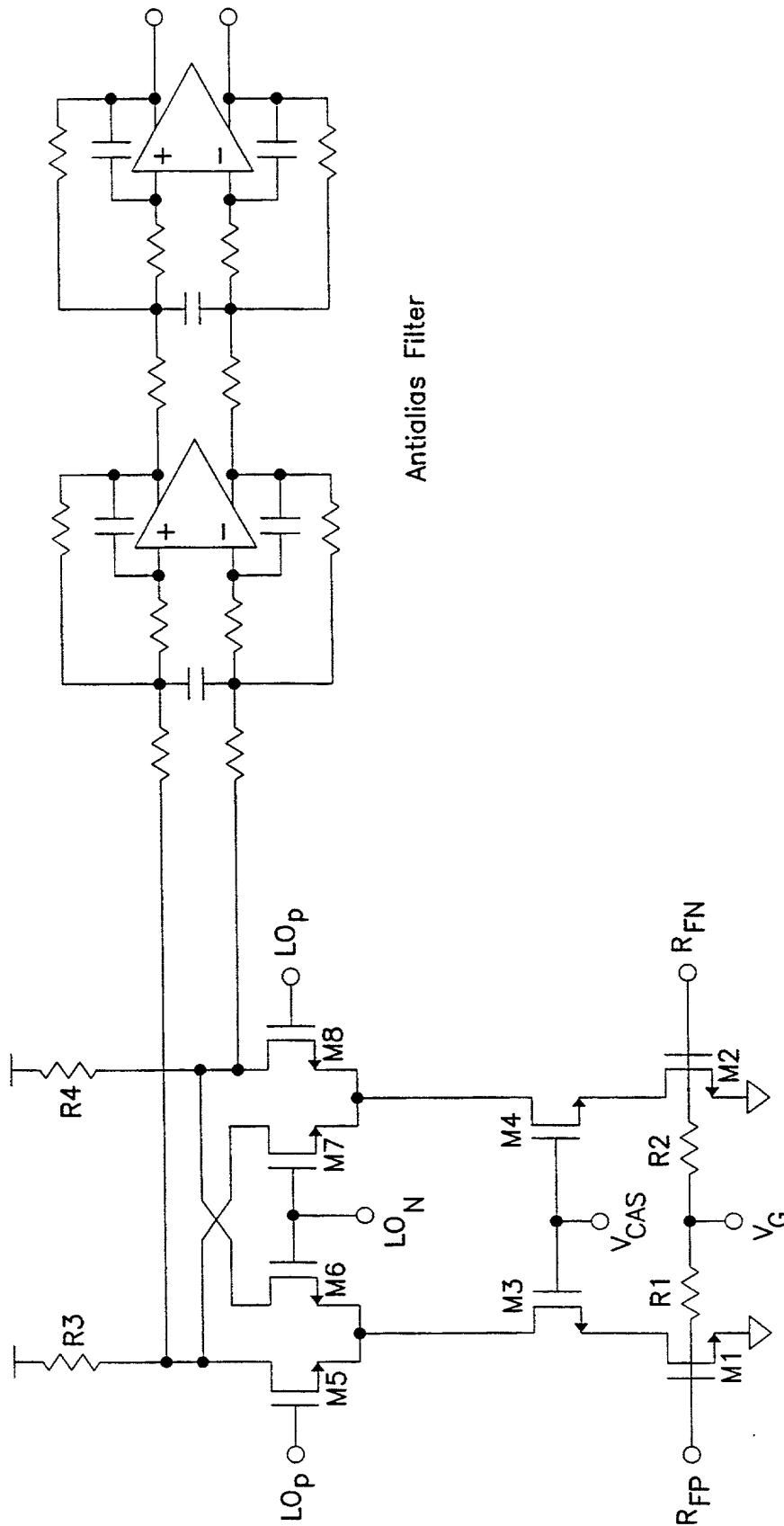


FIG. 3

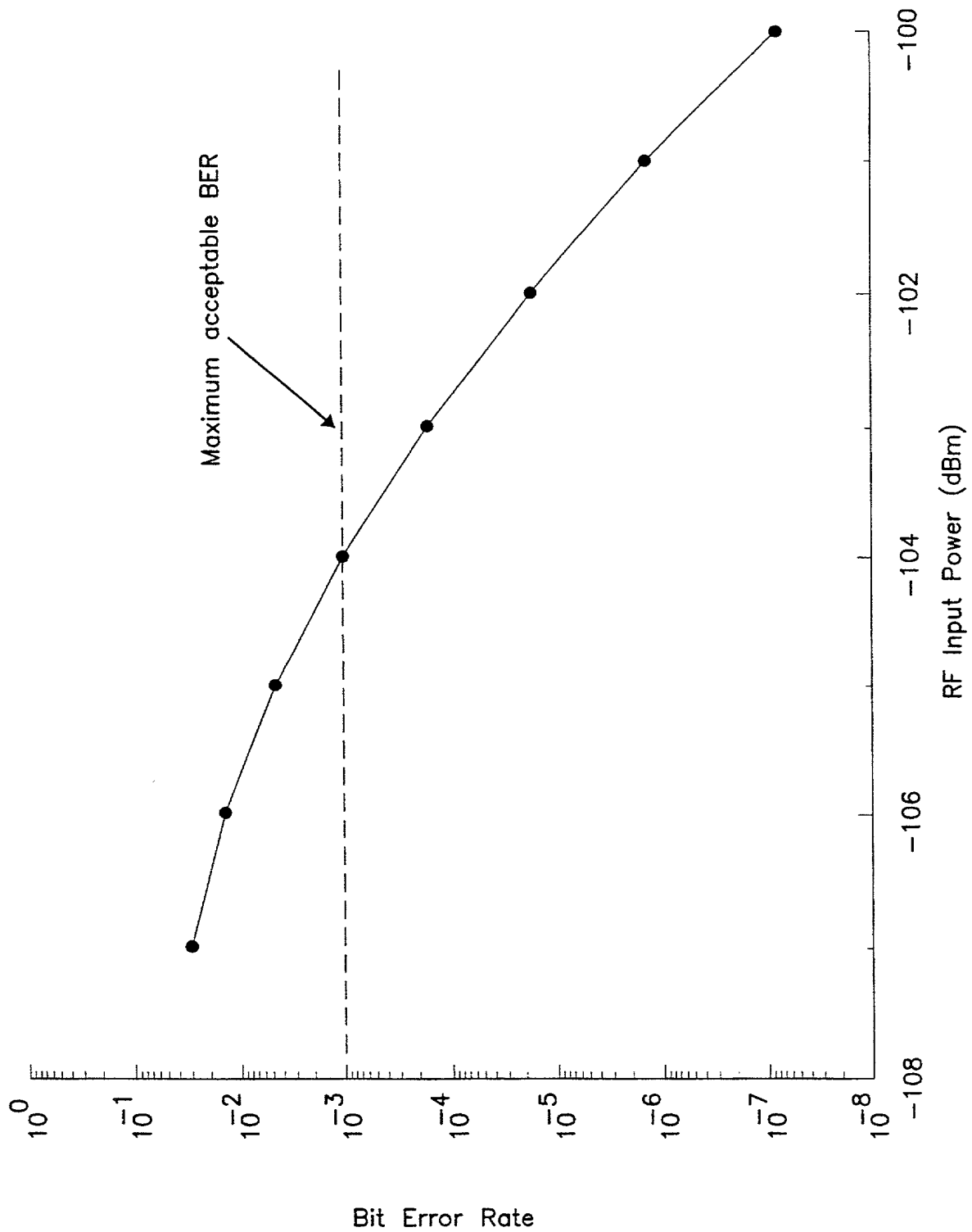


FIG. 4

FIG. 5

<u>Receiver</u>	
Sensitivity	-104dBm
Dynamic Range	110dB
Noise figure (DSB)	4.5dB
IIP2 (high gain)	+22dBm
IIP3 (high gain)	-21dBm
Selectivity (co-channel, 1.5MHz, 3MHz)	3dB, 23dB, 57dB
Blocking (4.5MHz)	67dB
Power dissipation (3.3V)	525mW
<u>Transmitter</u>	
Output power (into 50 Ω)	2, 8, 14, 20dBm
Bandwidth	1.5MHz
Modulation accuracy	$\pm 1\%$
Power dissipation (3.3V, 2dBm)	254mW
<u>General</u>	
Technology	0.6- μ m 2P3M CMOS
Die area	5.4mm x 6.7mm

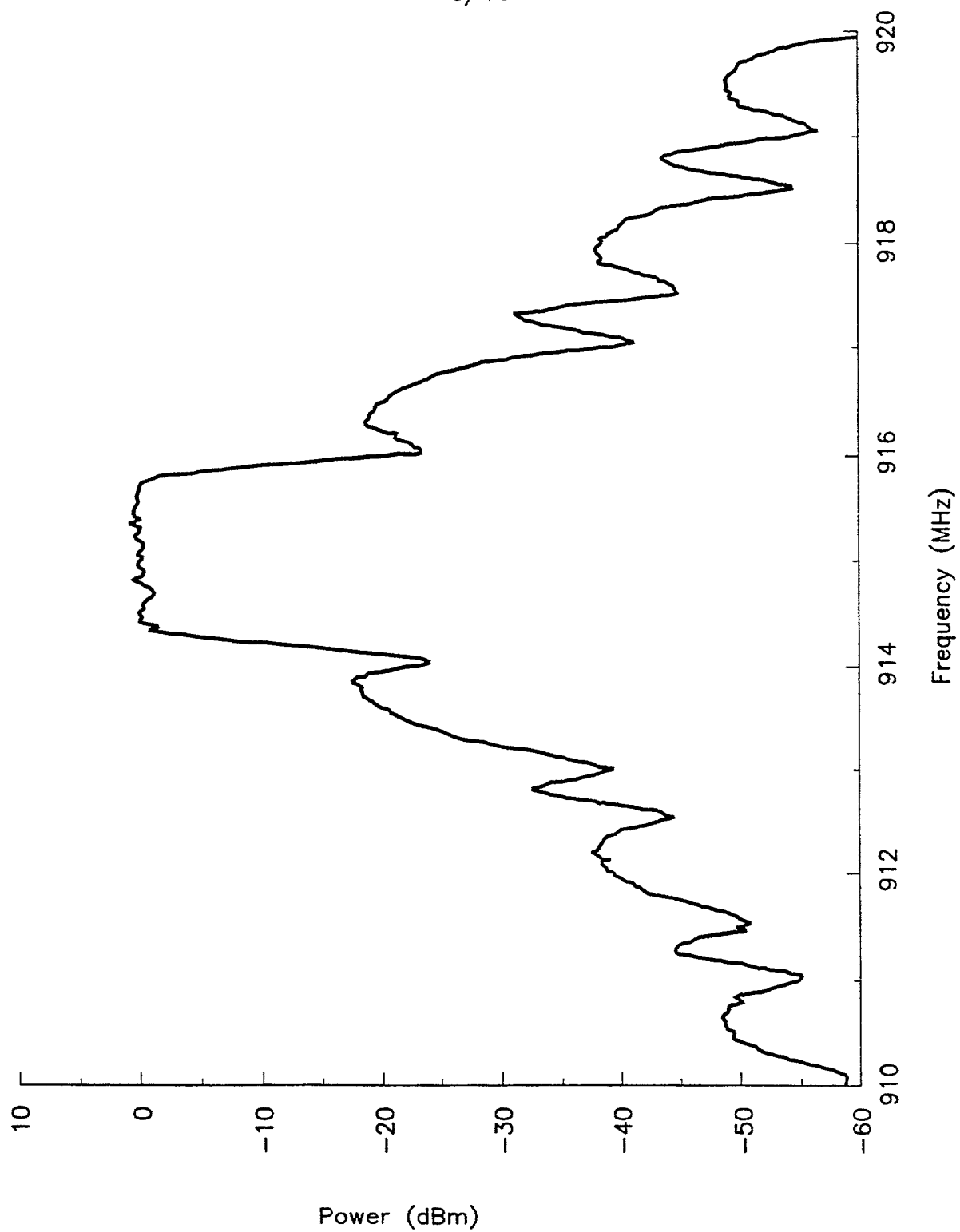
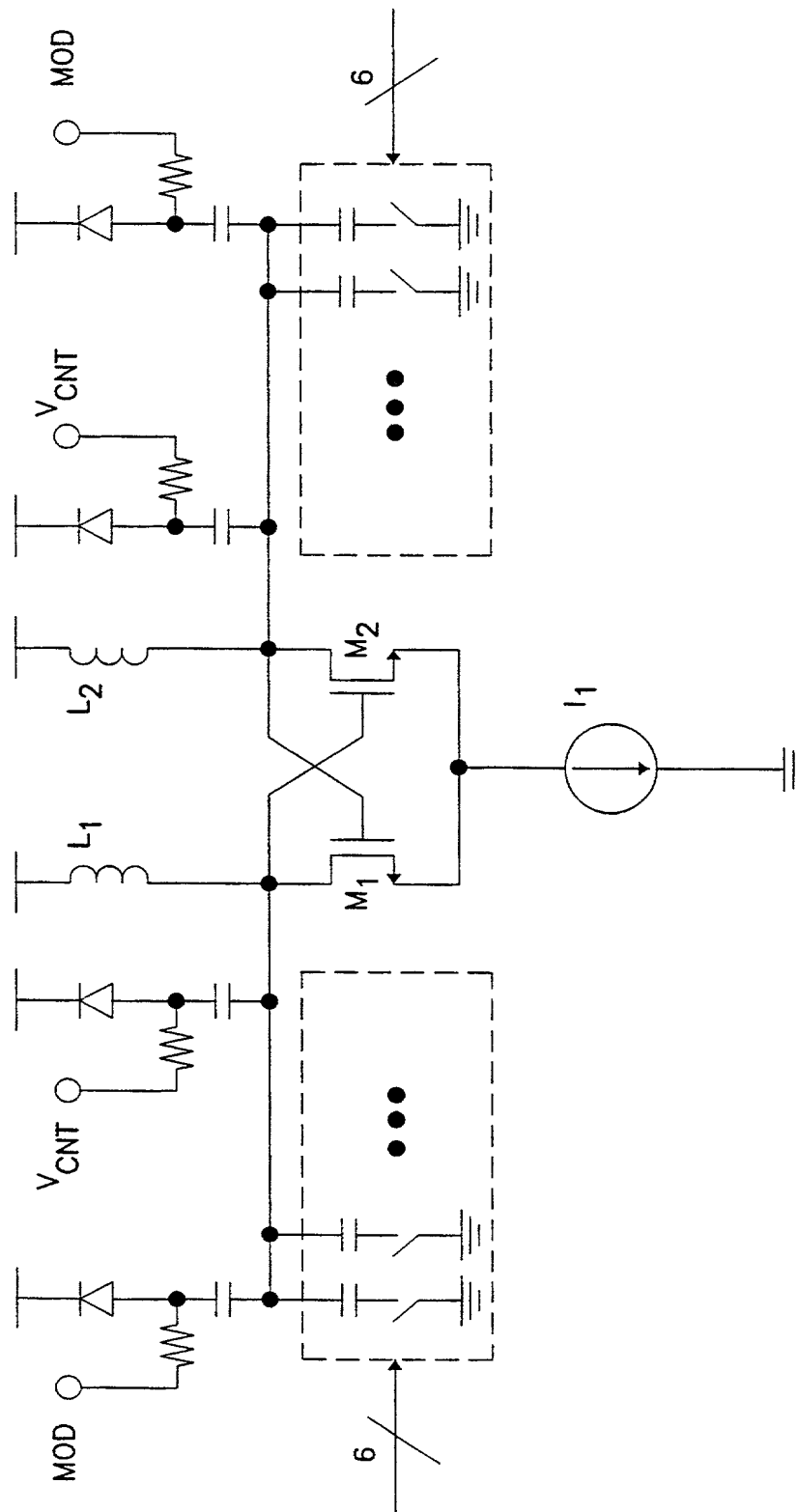


FIG. 6

FIG. 7



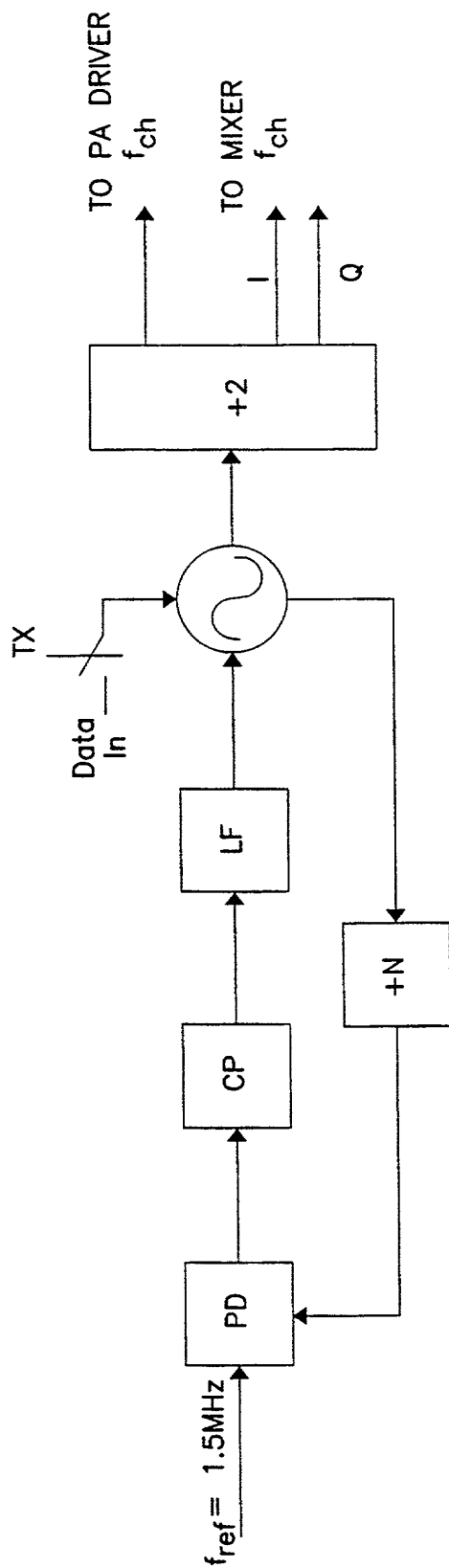


FIG. 8

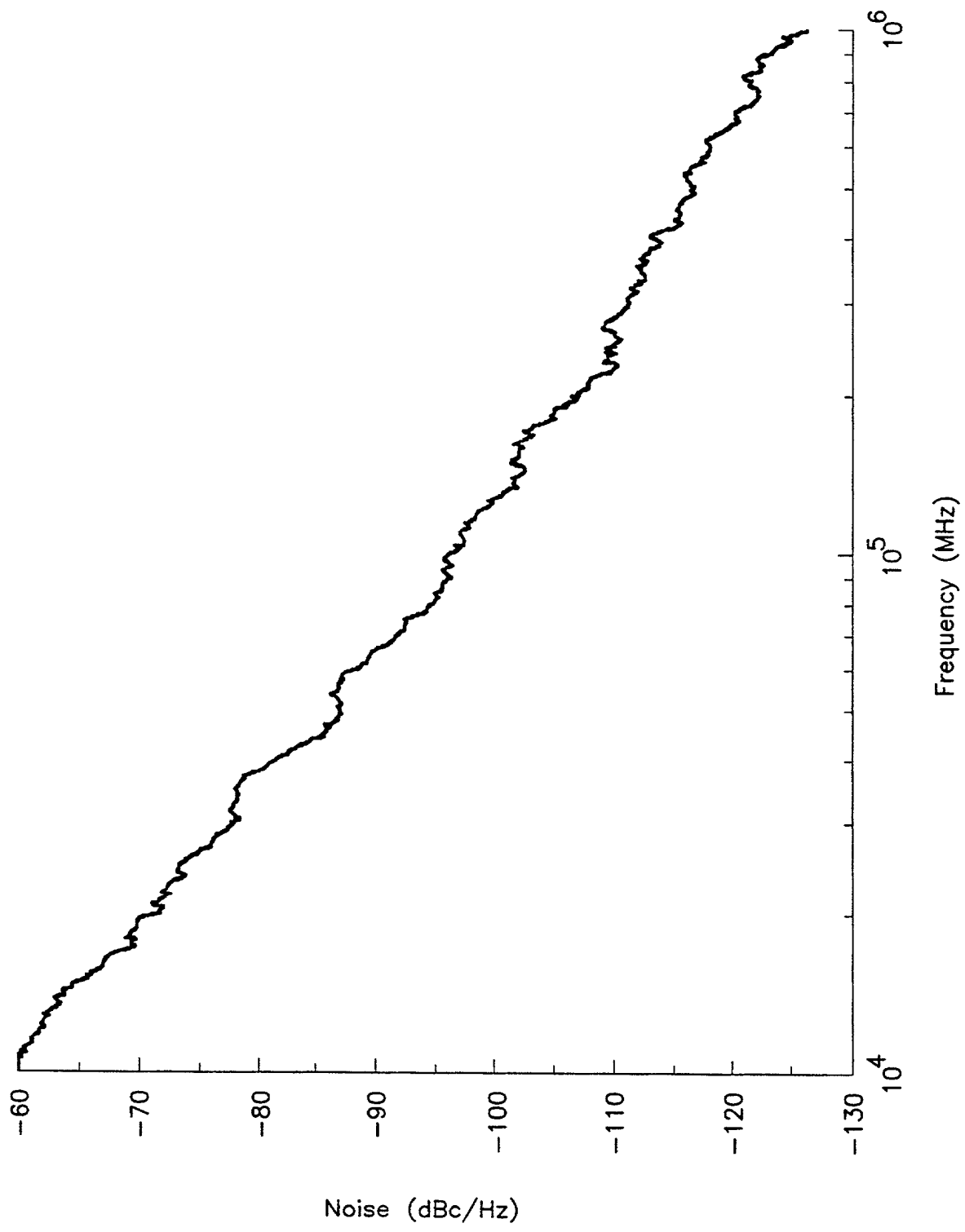


FIG. 9

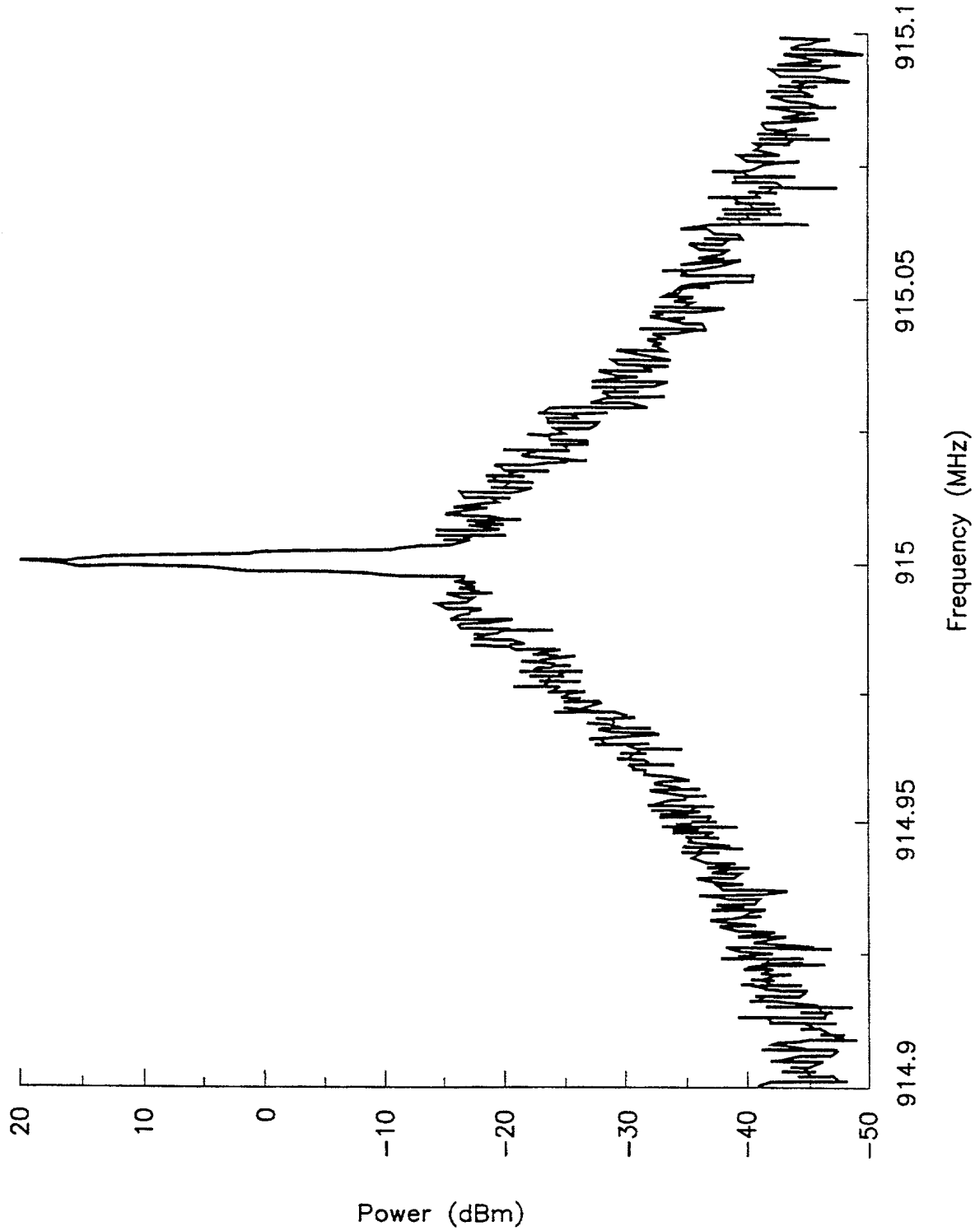


FIG. 10

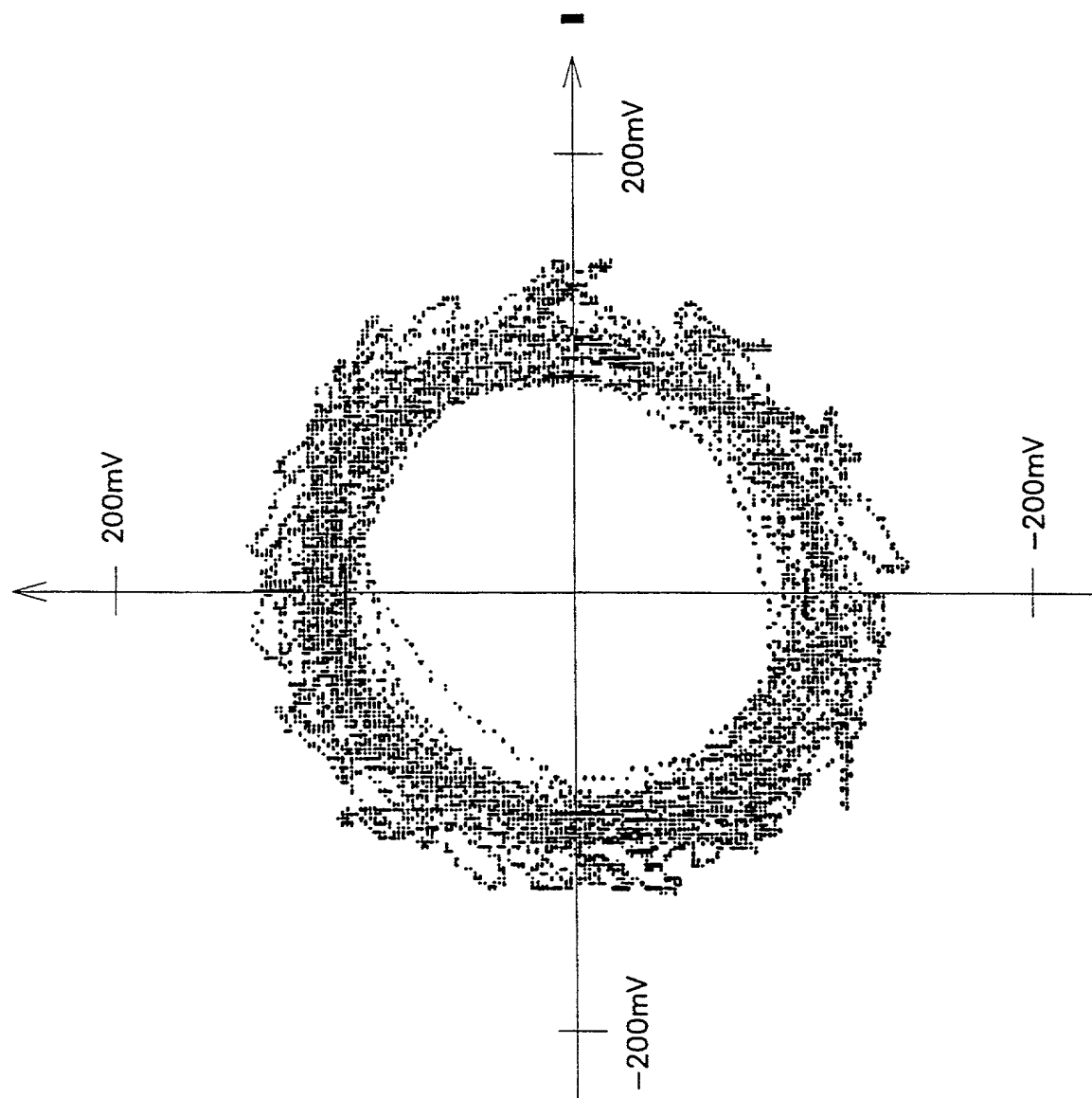
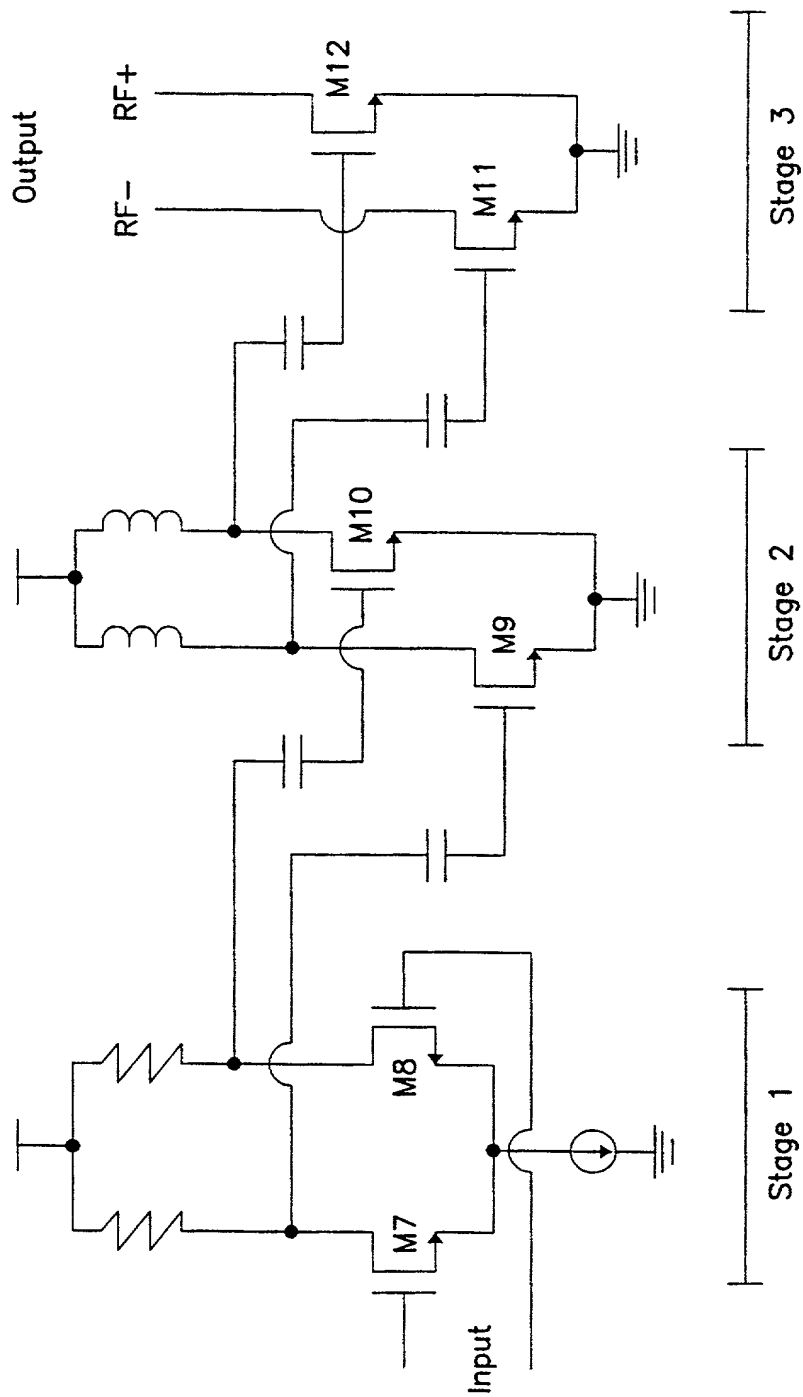


FIG. 11

FIG. 12



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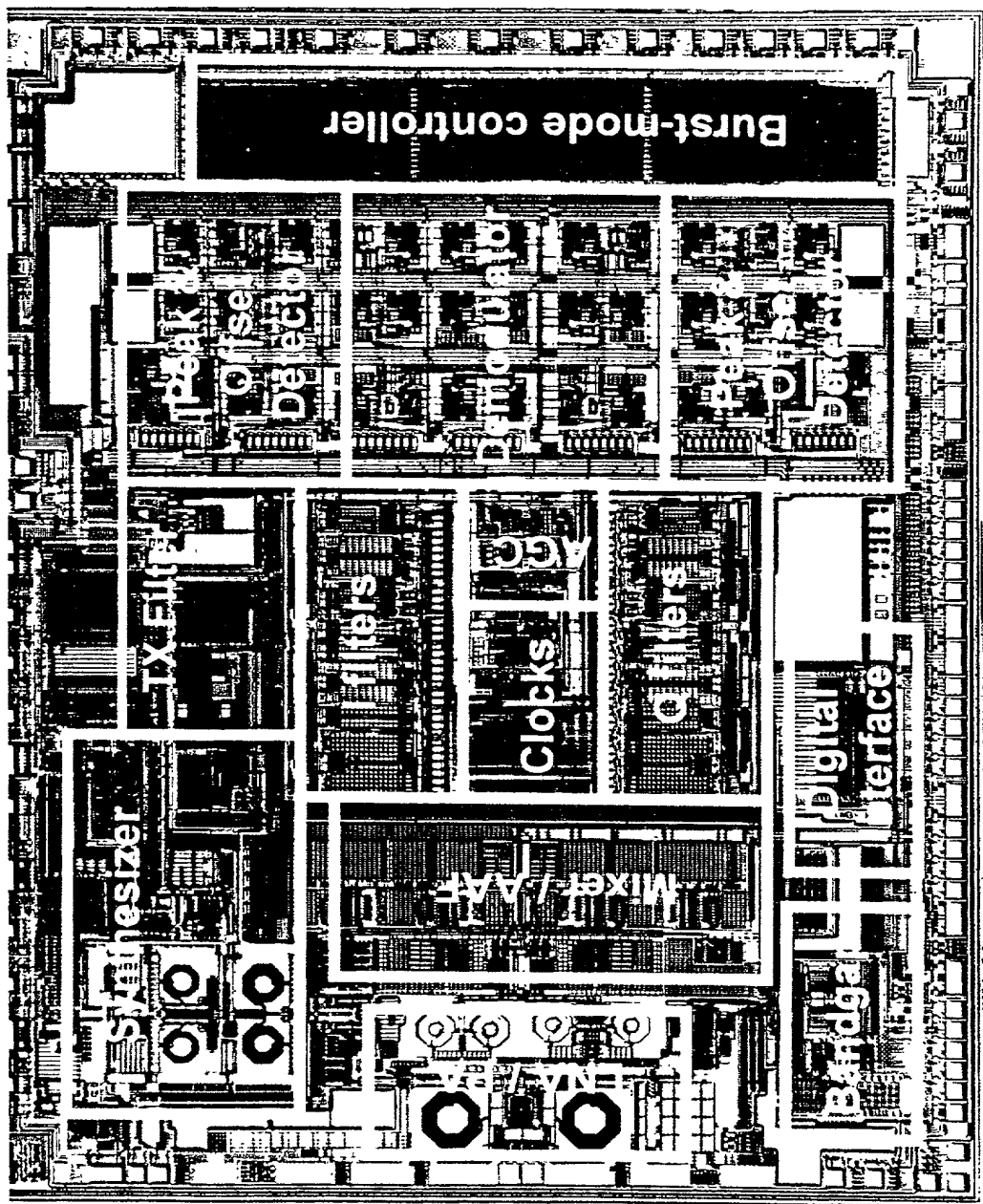


FIG. 13

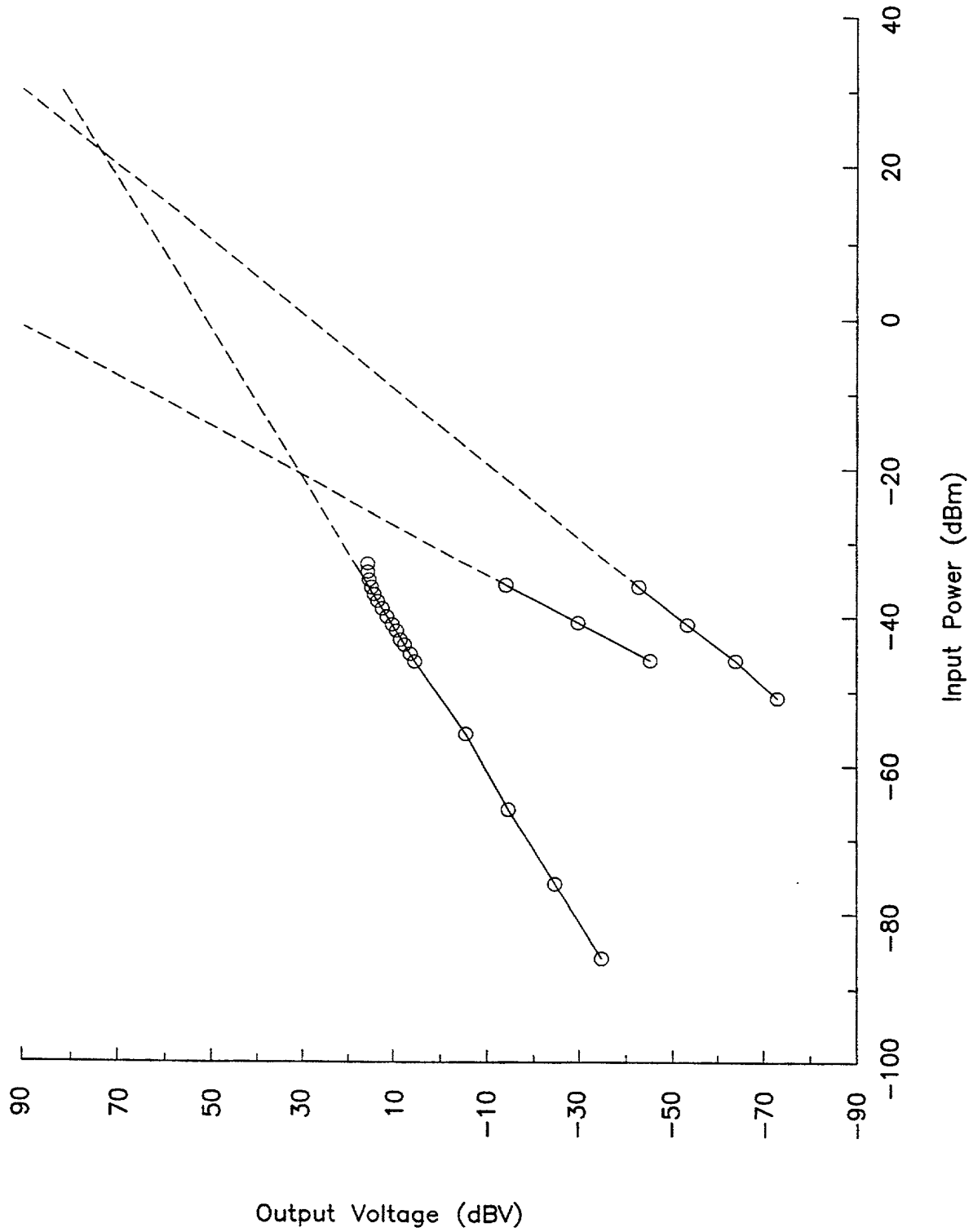


FIG. 14

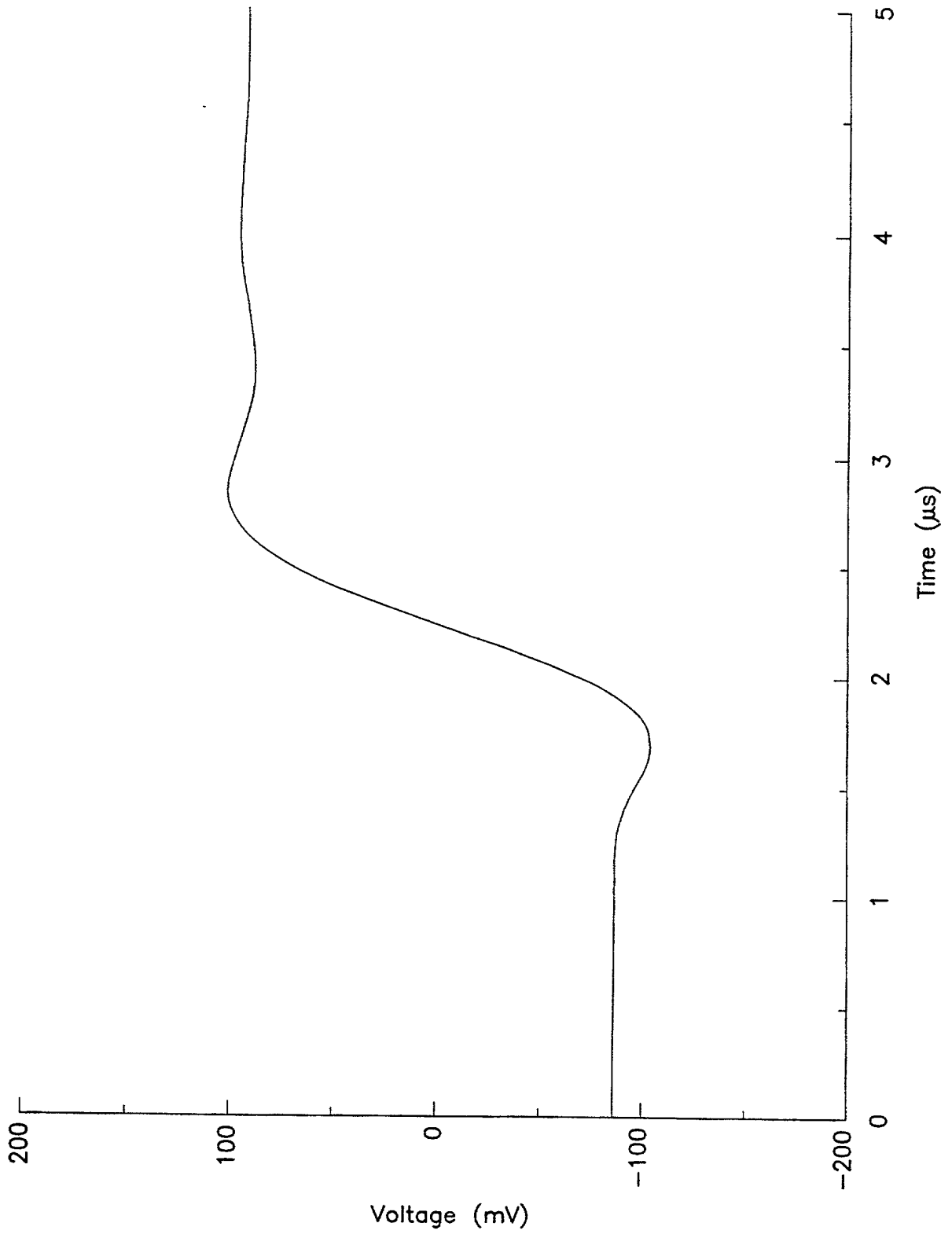
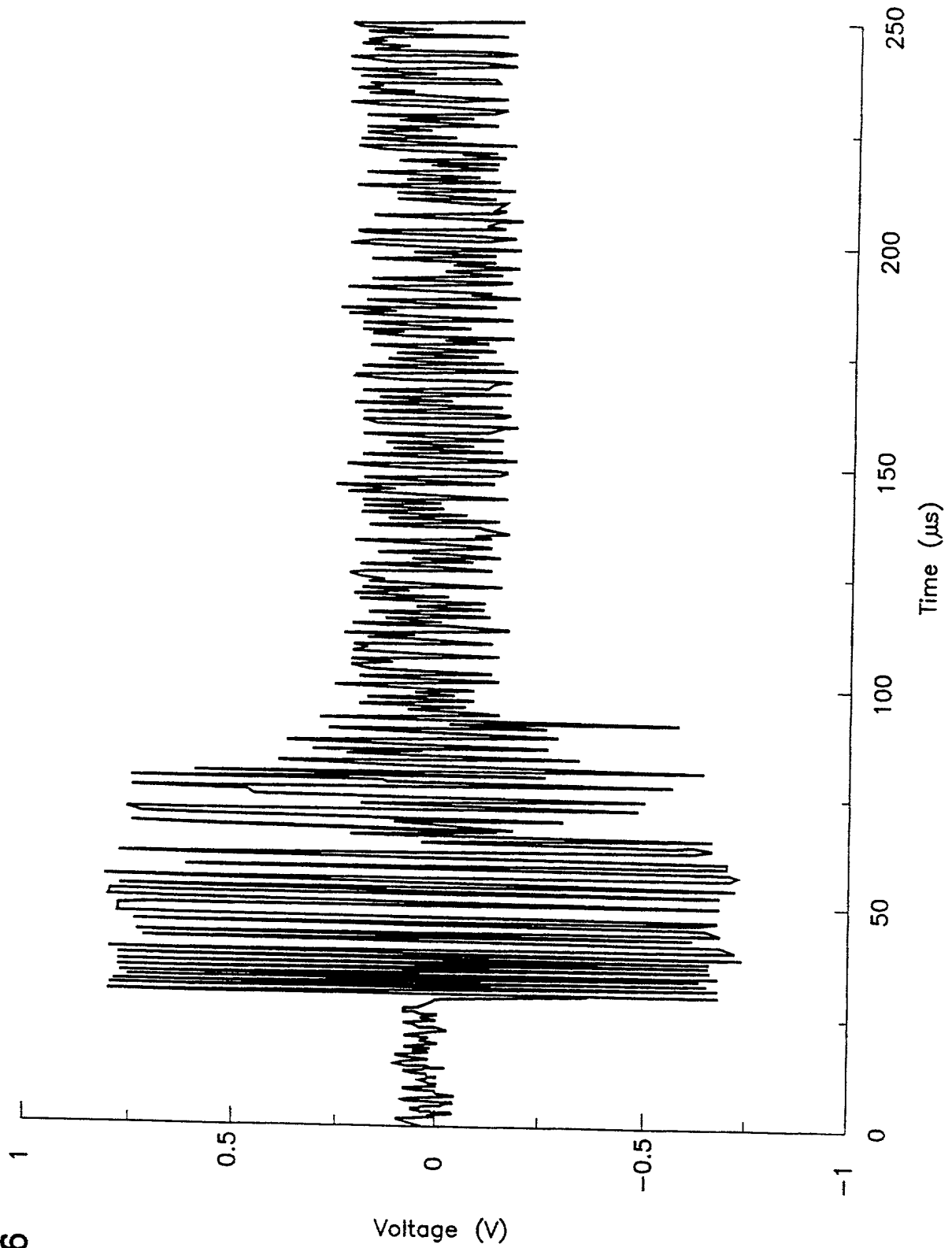


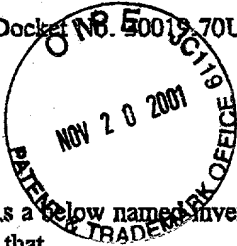
FIG. 15

FIG. 16



#8

Attorney Docket No. 50019-70USWO

MERCHANT & GOULD P.C.
United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

The specification of which

- a. ☐ is attached hereto
b. ☒ was filed on February 8, 2001 as application serial no. 09/762,720 and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. PCT/US99/20792 filed September 10, 1999, and as amended on September 27, 2000 (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

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I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

- a. ☒ no such applications have been filed.
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COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
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I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

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Signature of Inventor 208:			Date:	
2	Full Name Of Inventor	Family Name DUKATZ	First Given Name Eric	Second Given Name S.
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
9	Post Office Address	Post Office Address Apartment 2, 1012 Kirkham Street	City San Francisco	State & Zip Code/Country California 94122 U.S.A.
Signature of Inventor 209:			Date:	

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a

claim;

or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

MERCHANT & GOULD P.C.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

The specification of which

- a. ☐ is attached hereto
- b. ☒ was filed on February 8, 2001 as application serial no. 09/762,720 and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. PCT/US99/20792 filed September 10, 1999, and as amended on September 27, 2000 (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

- a. ☒ no such applications have been filed.
- b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (Day, Month, Year)
60/099,723	10 September 1998

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Albrecht, John W.	Reg. No. 40,481	Leonard, Christopher J.	Reg. No. 41,940
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Batzli, Brian H.	Reg. No. 32,960	Lycke, Lawrence E.	Reg. No. 38,540
Beard, John L.	Reg. No. 27,612	Mayfield, Denise L.	Reg. No. 33,732
Berns, John M.	Reg. No. 43,496	McDonald, Daniel W.	Reg. No. 32,044
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Bruess, Steven C.	Reg. No. 34,130	Nichols, A. Shane	Reg. No. 43,836
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Caspers, Philip P.	Reg. No. 33,227	Phillips, John B.	Reg. No. 37,206
Chiapetta, James R.	Reg. No. 39,634	Prendergast, Paul	Reg. No. 46,068
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Coldren, Richard J.	Reg. No. 44,084	Qualey, Terry	Reg. No. 25,148
Daignault, Ronald A.	Reg. No. 25,968	Reich, John C.	Reg. No. 37,703
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Dalglish, Leslie E.	Reg. No. 40,579	Roberts, Fred	Reg. No. 34,707
Daulton, Julie R.	Reg. No. 36,414	Samuels, Lisa A.	Reg. No. 43,080
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Gregson, Richard	Reg. No. 41,804	Swenson, Erik G.	Reg. No. 45,147
Gresens, John J.	Reg. No. 33,112	Tellekson, David K.	Reg. No. 32,314
Hamer, Samuel A.	Reg. No. 46,754	Trembath, Jon R.	Reg. No. 38,344
Hamre, Curtis B.	Reg. No. 29,165	Tuchman, Ido	Reg. No. 45,924
Harrison, Kevin C.	Reg. No. 46,759	Tunheim, Marcia A	Reg. No. 42,189
Hertzberg, Brett A.	Reg. No. 42,660	Underhill, Albert L.	Reg. No. 27,403
Hillson, Randall A.	Reg. No. 31,838	Vandenburgh, J. Derek	Reg. No. 32,179
Holzer, Jr., Richard J.	Reg. No. 42,668	Wahl, John R.	Reg. No. 33,044
Johnston, Scott W.	Reg. No. 39,721	Weaver, Karrie G.	Reg. No. 43,245
Kadievitch, Natalie D.	Reg. No. 34,196	Welter, Paul A.	Reg. No. 20,890
Karjeker, Shaukat	Reg. No. 34,049	Whipps, Brian	Reg. No. 43,261
Kettelberger, Denise	Reg. No. 33,924	Whitaker, John E.	Reg. No. 42,222
Keys, Jeramie J.	Reg. No. 42,724	Wickhem, J. Scot	Reg. No. 41,376
Knearl, Homer L.	Reg. No. 21,197	Williams, Douglas J.	Reg. No. 27,054
Kowalchyk, Alan W.	Reg. No. 31,535	Withers, James D.	Reg. No. 40,376
Kowalchyk, Katherine M.	Reg. No. 36,848	Witt, Jonelle	Reg. No. 41,980
Lacy, Paul E.	Reg. No. 38,946	Wu, Tong	Reg. No. 43,361
Larson, James A.	Reg. No. 40,443	Xu, Min S.	Reg. No. 39,536
Leon, Andrew J.	Reg. No. 46,869	Zeuli, Anthony R.	Reg. No. 45,255

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Merchant & Gould P.C. to the contrary.

Please direct all correspondence in this case to Merchant & Gould P.C. at the address indicated below:

Merchant & Gould P.C.
P.O. Box 2903
Minneapolis, MN 55402-0903

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2	Full Name Of Inventor	Family Name MACNALLY	First Given Name Donald	Second Given Name Evan
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
1	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 201:			Date:	
2	Full Name Of Inventor	Family Name CHO	First Given Name Thomas	Second Given Name B.
0	Residence & Citizenship	City Alameda	State or Foreign Country California	Country of Citizenship U.S.A. CA
2	Post Office Address	Post Office Address 356 Oleander Avenue	City Alameda	State & Zip Code/Country California 94502 U.S.A.
Signature of Inventor 202:			Date: 5/23/01	
2	Full Name Of Inventor	Family Name RABII	First Given Name Shahriar	Second Given Name
0	Residence & Citizenship	City Palo Alto	State or Foreign Country California	Country of Citizenship U.S.A.
3	Post Office Address	Post Office Address 2162 Stanton Court	City Palo Alto	State & Zip Code/Country California 94306 U.S.A.
Signature of Inventor 203:			Date:	
2	Full Name Of Inventor	Family Name MEHTA	First Given Name Srenik	Second Given Name Suresh
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
4	Post Office Address	Post Office Address 1468 8th Avenue	City San Francisco	State & Zip Code/Country California 94122 U.S.A.
Signature of Inventor 204:			Date:	
2	Full Name Of Inventor	Family Name NILSON	First Given Name Christopher	Second Given Name Donald
0	Residence & Citizenship	City San Jose	State or Foreign Country California	Country of Citizenship U.S.A.
5	Post Office Address	Post Office Address 170 South 14th Street	City San Jose	State & Zip Code/Country California 95112 U.S.A.
Signature of Inventor 205:			Date:	

2	Full Name Of Inventor	Family Name MACK	First Given Name Michael	Second Given Name Peter
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
6	Post Office Address	Post Office Address 3114 Clay Street #1	City San Francisco	State & Zip Code/Country California 94115 U.S.A.
Signature of Inventor 206:			Date:	
2	Full Name Of Inventor	Family Name PLOUVIER	First Given Name Laurence	Second Given Name Marguerite
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
7	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 207:			Date:	
2	Full Name Of Inventor	Family Name MARRINGA	First Given Name Menno	Second Given Name
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship Netherlands
8	Post Office Address	Post Office Address 25 Conrad Street	City San Francisco	State & Zip Code/Country California 94131 U.S.A.
Signature of Inventor 208:			Date:	
2	Full Name Of Inventor	Family Name DUKATZ	First Given Name Eric	Second Given Name S.
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
9	Post Office Address	Post Office Address Apartment 2, 1012 Kirkham Street	City San Francisco	State & Zip Code/Country California 94122 U.S.A.
Signature of Inventor 209:			Date:	

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(1) Each inventor named in the application:

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MERCHANT & GOULD P.C.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

The specification of which

- a. ☐ is attached hereto
b. ☒ was filed on February 8, 2001 as application serial no. 09/762,720 and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. PCT/US99/20792 filed September 10, 1999, and as amended on September 27, 2000 (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

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- a. ☒ no such applications have been filed.
b. ☐ such applications have been filed as follows:

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COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
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U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

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Daley, Dennis R.	Reg. No. 34,994	Reiland, Earl D.	Reg. No. 25,767
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Kettelberger, Denise	Reg. No. 33,924	Whitaker, John E.	Reg. No. 42,222
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Kowalchyk, Katherine M.	Reg. No. 36,848	Witt, Jonelle	Reg. No. 41,980
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Leon, Andrew J.	Reg. No. 46,869	Zeuli, Anthony R.	Reg. No. 45,255

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2	Full Name Of Inventor	Family Name MACNALLY	First Given Name Donald	Second Given Name Evan
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
1	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 201:			Date:	
2	Full Name Of Inventor	Family Name CHO	First Given Name Thomas	Second Given Name B.
0	Residence & Citizenship	City Alameda	State or Foreign Country California	Country of Citizenship U.S.A.
2	Post Office Address	Post Office Address 356 Oleander Avenue	City Alameda	State & Zip Code/Country California 94502 U.S.A.
Signature of Inventor 202:			Date:	
2	Full Name Of Inventor 3-00	Family Name RABII	First Given Name Shahriar	Second Given Name
0	Residence & Citizenship	City Palo Alto	State or Foreign Country California	Country of Citizenship U.S.A. CA
3	Post Office Address	Post Office Address 2162 Staunton Court 435 SHERIDAN AVE, #310	City Palo Alto	State & Zip Code/Country California 94306 U.S.A.
Signature of Inventor 203: <i>Shahriar Rabin</i>			Date: 4/19/2001	
2	Full Name Of Inventor 4-00	Family Name MEHTA	First Given Name Srenik	Second Given Name Suresh
0	Residence & Citizenship	City Pleasanton	State or Foreign Country California	Country of Citizenship U.S.A. CA
4	Post Office Address	Post Office Address 3543 Gresham Court	City Pleasanton	State & Zip Code/Country California 94588 U.S.A.
Signature of Inventor 204: X <i>Srenik Mehta</i>			Date: X 4/19/2001	
2	Full Name Of Inventor	Family Name NILSON	First Given Name Christopher	Second Given Name Donald
0	Residence & Citizenship	City San Jose	State or Foreign Country California	Country of Citizenship U.S.A.
5	Post Office Address	Post Office Address 170 South 14 th Street	City San Jose	State & Zip Code/Country California 95112 U.S.A.
Signature of Inventor 205:			Date:	

2	Full Name Of Inventor	Family Name MACK	First Given Name Michael	Second Given Name Peter
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
6	Post Office Address	Post Office Address 3114 Clay Street #1	City San Francisco	State & Zip Code/Country California 94115 U.S.A.
Signature of Inventor 206:				Date:
2	Full Name Of Inventor	Family Name PLOUVIER	First Given Name Laurence	Second Given Name Marguerite
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
7	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 207:				Date:
2	Full Name Of Inventor	Family Name MARRINGA	First Given Name Menno	Second Given Name
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship Netherlands
8	Post Office Address	Post Office Address 25 Conrad Street	City San Francisco	State & Zip Code/Country California 94131 U.S.A.
Signature of Inventor 208:				Date:
2	Full Name Of Inventor	Family Name DUKATZ	First Given Name Eric	Second Given Name S.
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
9	Post Office Address	Post Office Address Apartment 2, 1012 Kirkham Street	City San Francisco	State & Zip Code/Country California 94122 U.S.A.
Signature of Inventor 209:				Date:

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim;

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

MERCHANT & GOULD P.C.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

The specification of which

- a. ☐ is attached hereto
b. ☒ was filed on February 8, 2001 as application serial no. 09/762,720 and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. PCT/US99/20792 filed September 10, 1999, and as amended on September 27, 2000 (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

- a. ☒ no such applications have been filed.
b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (Day, Month, Year)
60/099,723	10 September 1998

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Albrecht, John W.	Reg. No. 40,481	Leonard, Christopher J.	Reg. No. 41,940
Ali, M. Jeffer	Reg. No. 46,359	Liepa, Mara E.	Reg. No. 40,066
Anderson, Gregg I.	Reg. No. 28,828	Lindquist, Timothy A.	Reg. No. 40,701
Batzli, Brian H.	Reg. No. 32,960	Lycke, Lawrence E.	Reg. No. 38,540
Beard, John L.	Reg. No. 27,612	Mayfield, Denise L.	Reg. No. 33,732
Berns, John M.	Reg. No. 43,496	McDonald, Daniel W.	Reg. No. 32,044
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Bruess, Steven C.	Reg. No. 34,130	Nichols, A. Shane	Reg. No. 43,836
Byrne, Linda M.	Reg. No. 32,404	Parsons, Nancy J.	Reg. No. 40,364
Campbell, Keith	Reg. No. 46,597	Pauly, Daniel M.	Reg. No. 40,123
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Caspers, Philip P.	Reg. No. 33,227	Phillips, John B.	Reg. No. 37,206
Chiapetta, James R.	Reg. No. 39,634	Prendergast, Paul	Reg. No. 46,068
Clifford, John A.	Reg. No. 30,247	Pytel, Melissa J.	Reg. No. 41,512
Coldren, Richard J.	Reg. No. 44,084	Qualey, Terry	Reg. No. 25,148
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Harrison, Kevin C.	Reg. No. 46,759	Tunheim, Marcia A.	Reg. No. 42,189
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Holzer, Jr., Richard J.	Reg. No. 42,668	Wahl, John R.	Reg. No. 33,044
Johnston, Scott W.	Reg. No. 39,721	Weaver, Karrie G.	Reg. No. 43,245
Kadievitch, Natalie D.	Reg. No. 34,196	Welter, Paul A.	Reg. No. 20,890
Karjeker, Shaukat	Reg. No. 34,049	Whipps, Brian	Reg. No. 43,261
Kettelberger, Denise	Reg. No. 33,924	Whitaker, John E.	Reg. No. 42,222
Keys, Jeramie J.	Reg. No. 42,724	Wickhem, J. Scot	Reg. No. 41,376
Knearl, Homer L.	Reg. No. 21,197	Williams, Douglas J.	Reg. No. 27,054
Kowalchyk, Alan W.	Reg. No. 31,535	Withers, James D.	Reg. No. 40,376
Kowalchyk, Katherine M.	Reg. No. 36,848	Witt, Jonelle	Reg. No. 41,980
Lacy, Paul E.	Reg. No. 38,946	Wu, Tong	Reg. No. 43,361
Larson, James A.	Reg. No. 40,443	Xu, Min S.	Reg. No. 39,536
Leon, Andrew J.	Reg. No. 46,869	Zeuli, Anthony R.	Reg. No. 45,255

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Merchant & Gould P.C. to the contrary.

Please direct all correspondence in this case to Merchant & Gould P.C. at the address indicated below:

Merchant & Gould P.C.
P.O. Box 2903
Minneapolis, MN 55402-0903

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2	Full Name Of Inventor	Family Name MACNALLY	First Given Name Donald	Second Given Name Evan
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
1	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 201:			Date:	
2	Full Name Of Inventor	Family Name CHO	First Given Name Thomas	Second Given Name B.
0	Residence & Citizenship	City Alameda	State or Foreign Country California	Country of Citizenship U.S.A.
2	Post Office Address	Post Office Address 356 Oleander Avenue	City Alameda	State & Zip Code/Country California 94502 U.S.A.
Signature of Inventor 202:			Date:	
2	Full Name Of Inventor	Family Name RABII	First Given Name Shahriar	Second Given Name
0	Residence & Citizenship	City Palo Alto	State or Foreign Country California	Country of Citizenship U.S.A.
3	Post Office Address	Post Office Address 2162 Staunton Court	City Palo Alto	State & Zip Code/Country California 94306 U.S.A.
Signature of Inventor 203:			Date:	
2	Full Name Of Inventor	Family Name MEHTA	First Given Name Srenik	Second Given Name Suresh
0	Residence & Citizenship	City Pleasanton	State or Foreign Country California	Country of Citizenship U.S.A.
4	Post Office Address	Post Office Address 3543 Gresham Court	City Pleasanton	State & Zip Code/Country California 94588 U.S.A.
Signature of Inventor 204:			Date:	
2	Full Name Of Inventor 5-00	Family Name NILSON	First Given Name Christopher	Second Given Name Donald
0	Residence & Citizenship	City San Jose	State or Foreign Country California	Country of Citizenship U.S.A. CH
5	Post Office Address	Post Office Address 170 South 14 th Street	City San Jose	State & Zip Code/Country California 95112 U.S.A.
Signature of Inventor 205:			Date: X 4/15/01	

2	Full Name Of Inventor	Family Name MACK	First Given Name Michael	Second Given Name Peter
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
6	Post Office Address	Post Office Address 3114 Clay Street #1	City San Francisco	State & Zip Code/Country California 94115 U.S.A.
Signature of Inventor 206:			Date:	
2	Full Name Of Inventor	Family Name PLOUVIER	First Given Name Laurence	Second Given Name Marguerite
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
7	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 207:			Date:	
2	Full Name Of Inventor	Family Name MARRINGA	First Given Name Menno	Second Given Name
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship Netherlands
8	Post Office Address	Post Office Address 25 Conrad Street	City San Francisco	State & Zip Code/Country California 94131 U.S.A.
Signature of Inventor 208:			Date:	
2	Full Name Of Inventor	Family Name DUKATZ	First Given Name Eric	Second Given Name S.
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
9	Post Office Address	Post Office Address Apartment 2, 1012 Kirkham Street	City San Francisco	State & Zip Code/Country California 94122 U.S.A.
Signature of Inventor 209:			Date:	

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

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(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a

claim;

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(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

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(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

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MERCHANT & GOULD P.C.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

The specification of which

- a. ☐ is attached hereto
b. ☒ was filed on February 8, 2001 as application serial no. 09/762,720 and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. PCT/US99/20792 filed September 10, 1999, and as amended on September 27, 2000 (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

- a. ☒ no such applications have been filed.
b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

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U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (Day, Month, Year)
60/099,723	10 September 1998

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

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Campbell, Keith	Reg. No. 46,597	Pauly, Daniel M.	Reg. No. 40,123
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Goggin, Matthew J.	Reg. No. 44,125	Skoog, Mark T.	Reg. No. 40,178
Golla, Charles E.	Reg. No. 26,896	Spellman, Steven J.	Reg. No. 45,124
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Leon, Andrew J.	Reg. No. 46,869	Zeuli, Anthony R.	Reg. No. 45,255

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Merchant & Gould P.C.
P.O. Box 2903
Minneapolis, MN 55402-0903

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2	Full Name Of Inventor	Family Name MACNALLY	First Given Name Donald	Second Given Name Evan
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
1	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 201:				Date:
2	Full Name Of Inventor	Family Name CHO	First Given Name Thomas	Second Given Name B.
0	Residence & Citizenship	City Alameda	State or Foreign Country California	Country of Citizenship U.S.A.
2	Post Office Address	Post Office Address 356 Oleander Avenue	City Alameda	State & Zip Code/Country California 94502 U.S.A.
Signature of Inventor 202:				Date:
2	Full Name Of Inventor	Family Name RABII	First Given Name Shahriar	Second Given Name
0	Residence & Citizenship	City Palo Alto	State or Foreign Country California	Country of Citizenship U.S.A.
3	Post Office Address	Post Office Address 2162 Staunton Court	City Palo Alto	State & Zip Code/Country California 94306 U.S.A.
Signature of Inventor 203:				Date:
2	Full Name Of Inventor	Family Name MEHTA	First Given Name Srenik	Second Given Name Suresh
0	Residence & Citizenship	City Pleasanton	State or Foreign Country California	Country of Citizenship U.S.A.
4	Post Office Address	Post Office Address 3543 Gresham Court	City Pleasanton	State & Zip Code/Country California 94588 U.S.A.
Signature of Inventor 204:				Date:
2	Full Name Of Inventor	Family Name NILSON	First Given Name Christopher	Second Given Name Donald
0	Residence & Citizenship	City San Jose	State or Foreign Country California	Country of Citizenship U.S.A.
5	Post Office Address	Post Office Address 170 South 14 th Street	City San Jose	State & Zip Code/Country California 95112 U.S.A.
Signature of Inventor 205:				Date:

2	Full Name Of Inventor <i>6-00</i>	Family Name MACK	First Given Name Michael	Second Given Name Peter
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A. <i>CA</i>
6	Post Office Address	Post Office Address 3114 Clay Street #1	City San Francisco	State & Zip Code/Country California 94115 U.S.A.
Signature of Inventor 206: <i>Michael P Mack</i>			Date: <i>April 11, 2001</i>	
2	Full Name Of Inventor	Family Name PLOUVIER	First Given Name Laurence	Second Given Name Marguerite
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
7	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 207:			Date:	
2	Full Name Of Inventor	Family Name MARRINGA	First Given Name Menno	Second Given Name
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship Netherlands
8	Post Office Address	Post Office Address 25 Conrad Street	City San Francisco	State & Zip Code/Country California 94131 U.S.A.
Signature of Inventor 208:			Date:	
2	Full Name Of Inventor	Family Name DUKATZ	First Given Name Eric	Second Given Name S.
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
9	Post Office Address	Post Office Address Apartment 2, 1012 Kirkham Street	City San Francisco	State & Zip Code/Country California 94122 U.S.A.
Signature of Inventor 209:			Date:	

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim;

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

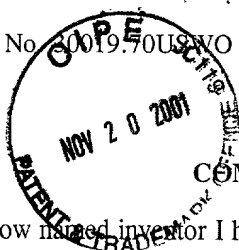
(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.



MERCHANT & GOULD P.C.

United States Patent Application

AS

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

The specification of which

- a. ☐ is attached hereto
 b. ☒ was filed on February 8, 2001 as application serial no. 09/762,720 and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. PCT/US99/20792 filed September 10, 1999, and as amended on September 27, 2000 (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

- a. ☒ no such applications have been filed.
 b. ☐ such applications have been filed as follows:

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NOV 2001

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

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NOV 29 2001

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, or abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (Day, Month, Year)
60/099,723	10 September 1998

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Albrecht, John W.	Reg. No. 40,481	Leonard, Christopher J.	Reg. No. 41,940
Ali, M. Jeffer	Reg. No. 46,359	Liepa, Mara E.	Reg. No. 40,066
Anderson, Gregg I.	Reg. No. 28,828	Lindquist, Timothy A.	Reg. No. 40,701
Batzli, Brian H.	Reg. No. 32,960	Lycke, Lawrence E.	Reg. No. 38,540
Beard, John L.	Reg. No. 27,612	Mayfield, Denise L.	Reg. No. 33,732
Berns, John M.	Reg. No. 43,496	McDonald, Daniel W.	Reg. No. 32,044
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Byrne, Linda M.	Reg. No. 32,404	Parsons, Nancy J.	Reg. No. 40,364
Campbell, Keith	Reg. No. 46,597	Pauly, Daniel M.	Reg. No. 40,123
Carlson, Alan G.	Reg. No. 25,959	Phillips, Bryan K.	Reg. No. 46,990
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Dalglish, Leslie E.	Reg. No. 40,579	Roberts, Fred	Reg. No. 34,707
Daulton, Julie R.	Reg. No. 36,414	Samuels, Lisa A.	Reg. No. 43,080
DeVries Smith, Katherine M.	Reg. No. 42,157	Schmaltz, David G.	Reg. No. 39,828
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Goggin, Matthew J.	Reg. No. 44,125	Skoog, Mark T.	Reg. No. 40,178
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Gresens, John J.	Reg. No. 33,112	Tellekson, David K.	Reg. No. 32,314
Hamer, Samuel A.	Reg. No. 46,754	Trembath, Jon R.	Reg. No. 38,344
Hamre, Curtis B.	Reg. No. 29,165	Tuchman, Ido	Reg. No. 45,924
Harrison, Kevin C.	Reg. No. 46,759	Tunheim, Marcia A	Reg. No. 42,189
Hertzberg, Brett A.	Reg. No. 42,660	Underhill, Albert L.	Reg. No. 27,403
Hillson, Randall A.	Reg. No. 31,838	Vandenburgh, J. Derek	Reg. No. 32,179
Holzer, Jr., Richard J.	Reg. No. 42,668	Wahl, John R.	Reg. No. 33,044
Johnston, Scott W.	Reg. No. 39,721	Weaver, Karrie G.	Reg. No. 43,245
Kadievitch, Natalie D.	Reg. No. 34,196	Welter, Paul A.	Reg. No. 20,890
Karjeker, Shaukat	Reg. No. 34,049	Whipps, Brian	Reg. No. 43,261
Kettelberger, Denise	Reg. No. 33,924	Whitaker, John E.	Reg. No. 42,222
Keys, Jeramie J.	Reg. No. 42,724	Wickhem, J. Scot	Reg. No. 41,376
Knearl, Homer L.	Reg. No. 21,197	Williams, Douglas J.	Reg. No. 27,054
Kowalchyk, Alan W.	Reg. No. 31,535	Withers, James D.	Reg. No. 40,376
Kowalchyk, Katherine M.	Reg. No. 36,848	Witt, Jonelle	Reg. No. 41,980
Lacy, Paul E.	Reg. No. 38,946	Wu, Tong	Reg. No. 43,361
Larson, James A.	Reg. No. 40,443	Xu, Min S.	Reg. No. 39,536
Leon, Andrew J.	Reg. No. 46,869	Zeuli, Anthony R.	Reg. No. 45,255

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Merchant & Gould P.C. to the contrary.

Please direct all correspondence in this case to Merchant & Gould P.C. at the address indicated below:

Merchant & Gould P.C.
P.O. Box 2903
Minneapolis, MN 55402-0903

RECEIVED

NOV 29 2001

OFFICE OF PETITIONS
DEPUTY A/C PATENTS

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.


2	Full Name Of Inventor	Family Name MACNALLY	First Given Name Donald	Second Given Name Evan
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
1	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 201:			Date:	

2	Full Name Of Inventor	Family Name CHO	First Given Name Thomas	Second Given Name B.
0	Residence & Citizenship	City Alameda	State or Foreign Country California	Country of Citizenship U.S.A.
2	Post Office Address	Post Office Address 356 Oleander Avenue	City Alameda	State & Zip Code/Country California 94502 U.S.A.
Signature of Inventor 202:			Date:	

2	Full Name Of Inventor	Family Name RABII	First Given Name Shahriar	Second Given Name
0	Residence & Citizenship	City Palo Alto	State or Foreign Country California	Country of Citizenship U.S.A.
3	Post Office Address	Post Office Address 2162 Staunton Court	City Palo Alto	State & Zip Code/Country California 94306 U.S.A.
Signature of Inventor 203:			Date:	

2	Full Name Of Inventor	Family Name MEHTA	First Given Name Srenik	Second Given Name Suresh
0	Residence & Citizenship	City Pleasanton	State or Foreign Country California	Country of Citizenship U.S.A.
4	Post Office Address	Post Office Address 3543 Gresham Court	City Pleasanton	State & Zip Code/Country California 94588 U.S.A.
Signature of Inventor 204:			Date:	

2	Full Name Of Inventor	Family Name NILSON	First Given Name Christopher	Second Given Name Donald
0	Residence & Citizenship	City San Jose	State or Foreign Country California	Country of Citizenship U.S.A.
5	Post Office Address	Post Office Address 170 South 14 th Street	City San Jose	State & Zip Code/Country California 95112 U.S.A.
Signature of Inventor 205:			Date:	

2	Full Name Of Inventor	Family Name MACK	First Given Name Michael	Second Given Name Peter
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
6	Post Office Address	Post Office Address 3114 Clay Street #1	City San Francisco	State & Zip Code/Country California 94115 U.S.A.
Signature of Inventor 206:			Date:	
2	Full Name Of Inventor 7-00	Family Name PLOUVIER	First Given Name Laurence	Second Given Name Marguerite
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A. CA
7	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 207: 			Date: X October 29 th 2001	
2	Full Name Of Inventor	Family Name MARRINGA	First Given Name Menno	Second Given Name
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship Netherlands
8	Post Office Address	Post Office Address 25 Conrad Street	City San Francisco	State & Zip Code/Country California 94131 U.S.A.
Signature of Inventor 208:			Date:	
2	Full Name Of Inventor	Family Name DUKATZ	First Given Name Eric	Second Given Name S.
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
9	Post Office Address	Post Office Address Apartment 2, 1012 Kirkham Street	City San Francisco	State & Zip Code/Country California 94122 U.S.A.
Signature of Inventor 209:			Date:	

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

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(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

MERCHANT & GOULD P.C.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

The specification of which

- a. ☐ is attached hereto
- b. ☒ was filed on February 8, 2001 as application serial no. 09/762,720 and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. PCT/US99/20792 filed September 10, 1999, and as amended on September 27, 2000 (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

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- a. ☒ no such applications have been filed.
- b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

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U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

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Coldren, Richard J.	Reg. No. 44,084	Qualey, Terry	Reg. No. 25,148
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Hammer, Samuel A.	Reg. No. 46,754	Trembath, Jon R.	Reg. No. 38,344
Hamre, Curtis B.	Reg. No. 29,165	Tuchman, Ido	Reg. No. 45,924
Harrison, Kevin C.	Reg. No. 46,759	Tunheim, Marcia A.	Reg. No. 42,189
Hertzberg, Brett A.	Reg. No. 42,660	Underhill, Albert L.	Reg. No. 27,403
Hillson, Randall A.	Reg. No. 31,838	Vandenburgh, J. Derek	Reg. No. 32,179
Holzer, Jr., Richard J.	Reg. No. 42,668	Wahl, John R.	Reg. No. 33,044
Johnston, Scott W.	Reg. No. 39,721	Weaver, Karrie G.	Reg. No. 43,245
Kadievitch, Natalie D.	Reg. No. 34,196	Welter, Paul A.	Reg. No. 20,890
Karjeker, Shaikat	Reg. No. 34,049	Whipps, Brian	Reg. No. 43,261
Kettelberger, Denise	Reg. No. 33,924	Whitaker, John E.	Reg. No. 42,222
Keys, Jeramie J.	Reg. No. 42,724	Wickhem, J. Scot	Reg. No. 41,376
Knearl, Homer L.	Reg. No. 21,197	Williams, Douglas J.	Reg. No. 27,054
Kowalchuk, Alan W.	Reg. No. 31,535	Withers, James D.	Reg. No. 40,376
Kowalchuk, Katherine M.	Reg. No. 36,848	Witt, Jonelle	Reg. No. 41,980
Lacy, Paul E.	Reg. No. 38,946	Wu, Tong	Reg. No. 43,361
Larson, James A.	Reg. No. 40,443	Xu, Min S.	Reg. No. 39,536
Leon, Andrew J.	Reg. No. 46,869	Zeuli, Anthony R.	Reg. No. 45,255

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Merchant & Gould P.C. to the contrary.

Please direct all correspondence in this case to Merchant & Gould P.C. at the address indicated below:

Merchant & Gould P.C.
P.O. Box 2903
Minneapolis, MN 55402-0903

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2	Full Name Of Inventor	Family Name MACNALLY	First Given Name Donald	Second Given Name Evan
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
1	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 201:			Date:	
2	Full Name Of Inventor	Family Name CHO	First Given Name Thomas	Second Given Name B.
0	Residence & Citizenship	City Alameda	State or Foreign Country California	Country of Citizenship U.S.A.
2	Post Office Address	Post Office Address 356 Oleander Avenue	City Alameda	State & Zip Code/Country California 94502 U.S.A.
Signature of Inventor 202:			Date:	
2	Full Name Of Inventor	Family Name RABII	First Given Name Shahriar	Second Given Name
0	Residence & Citizenship	City Palo Alto	State or Foreign Country California	Country of Citizenship U.S.A.
3	Post Office Address	Post Office Address 2162 Staunton Court	City Palo Alto	State & Zip Code/Country California 94306 U.S.A.
Signature of Inventor 203:			Date:	
2	Full Name Of Inventor	Family Name MEHTA	First Given Name Srenik	Second Given Name Suresh
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Signature of Inventor 204:			Date:	
2	Full Name Of Inventor	Family Name NILSON	First Given Name Christopher	Second Given Name Donald
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5	Post Office Address	Post Office Address 170 South 14 th Street	City San Jose	State & Zip Code/Country California 95112 U.S.A.
Signature of Inventor 205:			Date:	

2	Full Name Of Inventor	Family Name MACK	First Given Name Michael	Second Given Name Peter
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6	Post Office Address	Post Office Address 3114 Clay Street #1	City San Francisco	State & Zip Code/Country California 94115 U.S.A.
Signature of Inventor 206:			Date:	
2	Full Name Of Inventor	Family Name PLOUVIER	First Given Name Laurence	Second Given Name Marguerite
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
7	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 207:			Date:	
2	Full Name Of Inventor 8-00	Family Name <u>MARRINGA</u>	First Given Name <u>Menno</u>	Second Given Name <u>CA</u>
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship Netherlands
8	Post Office Address	Post Office Address 25 Conrad Street	City San Francisco	State & Zip Code/Country California 94131 U.S.A.
Signature of Inventor 208:			Date: X 16 APRIL 2001	
2	Full Name Of Inventor	Family Name DUKATZ	First Given Name Eric	Second Given Name S.
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
9	Post Office Address	Post Office Address Apartment 2, 1012 Kirkham Street	City San Francisco	State & Zip Code/Country California 94122 U.S.A.
Signature of Inventor 209:			Date:	

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim;

or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

MERCHANT & GOULD P.C.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

The specification of which

- a. ☐ is attached hereto
- b. ☒ was filed on February 8, 2001 as application serial no. 09/762,720 and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. PCT/US99/20792 filed September 10, 1999, and as amended on September 27, 2000 (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

- a. ☒ no such applications have been filed.
- b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (Day, Month, Year)
60/099,723	10 September 1998

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

TOP SECRET

Albrecht, John W.	Reg. No. 40,481	Leonard, Christopher J.	Reg. No. 41,940
Ali, M. Jeffer	Reg. No. 46,359	Liepa, Mara E.	Reg. No. 40,066
Anderson, Gregg I.	Reg. No. 28,828	Lindquist, Timothy A.	Reg. No. 40,701
Batzli, Brian H.	Reg. No. 32,960	Lycke, Lawrence E.	Reg. No. 38,540
Beard, John L.	Reg. No. 27,612	Mayfield, Denise L.	Reg. No. 33,732
Berns, John M.	Reg. No. 43,496	McDonald, Daniel W.	Reg. No. 32,044
Black, Bruce E.	Reg. No. 41,622	McIntyre, Jr., William F.	Reg. No. 44,921
Branch, John W.	Reg. No. 41,633	Mitchem, M. Todd	Reg. No. 40,731
Bremer, Dennis C.	Reg. No. 40,528	Mueller, Douglas P.	Reg. No. 30,300
Bruess, Steven C.	Reg. No. 34,130	Nichols, A. Shane	Reg. No. 43,836
Byrne, Linda M.	Reg. No. 32,404	Parsons, Nancy J.	Reg. No. 40,364
Campbell, Keith	Reg. No. 46,597	Pauly, Daniel M.	Reg. No. 40,123
Carlson, Alan G.	Reg. No. 25,959	Phillips, Bryan K.	Reg. No. 46,990
Caspers, Philip P.	Reg. No. 33,227	Phillips, John B.	Reg. No. 37,206
Chiapetta, James R.	Reg. No. 39,634	Prendergast, Paul	Reg. No. 46,068
Clifford, John A.	Reg. No. 30,247	Pytel, Melissa J.	Reg. No. 41,512
Coldren, Richard J.	Reg. No. 44,084	Qualey, Terry	Reg. No. 25,148
Daignault, Ronald A.	Reg. No. 25,968	Reich, John C.	Reg. No. 37,703
Daley, Dennis R.	Reg. No. 34,994	Reiland, Earl D.	Reg. No. 25,767
Dalglish, Leslie E.	Reg. No. 40,579	Roberts, Fred	Reg. No. 34,707
Daulton, Julie R.	Reg. No. 36,414	Samuels, Lisa A.	Reg. No. 43,080
DeVries Smith, Katherine M.	Reg. No. 42,157	Schmaltz, David G.	Reg. No. 39,828
DiPietro, Mark J.	Reg. No. 28,707	Schuman, Mark D.	Reg. No. 31,197
Edell, Robert T.	Reg. No. 20,187	Schumann, Michael D.	Reg. No. 30,422
Epp Ryan, Sandra	Reg. No. 39,667	Scull, Timothy B.	Reg. No. 42,137
Glance, Robert J.	Reg. No. 40,620	Sebald, Gregory A.	Reg. No. 33,280
Goggin, Matthew J.	Reg. No. 44,125	Skoog, Mark T.	Reg. No. 40,178
Golla, Charles E.	Reg. No. 26,896	Spellman, Steven J.	Reg. No. 45,124
Gorman, Alan G.	Reg. No. 38,472	Stall-DeBell, Kirstin L.	Reg. No. 43,164
Gould, John D.	Reg. No. 18,223	Sumner, John P.	Reg. No. 29,114
Gregson, Richard	Reg. No. 41,804	Swenson, Erik G.	Reg. No. 45,147
Gresens, John J.	Reg. No. 33,112	Tellekson, David K.	Reg. No. 32,314
Hamer, Samuel A.	Reg. No. 46,754	Trembath, Jon R.	Reg. No. 38,344
Hamre, Curtis B.	Reg. No. 29,165	Tuchman, Ido	Reg. No. 45,924
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Hertzberg, Brett A.	Reg. No. 42,660	Underhill, Albert L.	Reg. No. 27,403
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Karjeker, Shaukat	Reg. No. 34,049	Whipps, Brian	Reg. No. 43,261
Kettelberger, Denise	Reg. No. 33,924	Whitaker, John E.	Reg. No. 42,222
Keys, Jeraime J.	Reg. No. 42,724	Wickhem, J. Scot	Reg. No. 41,376
Knearl, Homer L.	Reg. No. 21,197	Williams, Douglas J.	Reg. No. 27,054
Kowalchuk, Alan W.	Reg. No. 31,535	Withers, James D.	Reg. No. 40,376
Kowalchuk, Katherine M.	Reg. No. 36,848	Witt, Jonelle	Reg. No. 41,980
Lacy, Paul E.	Reg. No. 38,946	Wu, Tong	Reg. No. 43,361
Larson, James A.	Reg. No. 40,443	Xu, Min S.	Reg. No. 39,536
Leon, Andrew J.	Reg. No. 46,869	Zeuli, Anthony R.	Reg. No. 45,255

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Merchant & Gould P.C. to the contrary.

Please direct all correspondence in this case to Merchant & Gould P.C. at the address indicated below:

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Minneapolis, MN 55402-0903

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2	Full Name Of Inventor	Family Name MACNALLY	First Given Name Donald	Second Given Name Evan
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
1	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 201:				Date:
2	Full Name Of Inventor	Family Name CHO	First Given Name Thomas	Second Given Name B.
0	Residence & Citizenship	City Alameda	State or Foreign Country California	Country of Citizenship U.S.A.
2	Post Office Address	Post Office Address 356 Oleander Avenue	City Alameda	State & Zip Code/Country California 94502 U.S.A.
Signature of Inventor 202:				Date:
2	Full Name Of Inventor	Family Name RABII	First Given Name Shahriar	Second Given Name
0	Residence & Citizenship	City Palo Alto	State or Foreign Country California	Country of Citizenship U.S.A.
3	Post Office Address	Post Office Address 2162 Staunton Court	City Palo Alto	State & Zip Code/Country California 94306 U.S.A.
Signature of Inventor 203:				Date:
2	Full Name Of Inventor	Family Name MEHTA	First Given Name Srenik	Second Given Name Suresh
0	Residence & Citizenship	City Pleasanton	State or Foreign Country California	Country of Citizenship U.S.A.
4	Post Office Address	Post Office Address 3543 Gresham Court	City Pleasanton	State & Zip Code/Country California 94588 U.S.A.
Signature of Inventor 204:				Date:
2	Full Name Of Inventor	Family Name NILSON	First Given Name Christopher	Second Given Name Donald
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5	Post Office Address	Post Office Address 170 South 14 th Street	City San Jose	State & Zip Code/Country California 95112 U.S.A.
Signature of Inventor 205:				Date:

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Signature of Inventor 206:			Date:	
2	Full Name Of Inventor	Family Name PLOUVIER	First Given Name Laurence	Second Given Name Marguerite
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7	Post Office Address	Post Office Address 141 Bronte Street	City San Francisco	State & Zip Code/Country California 94110 U.S.A.
Signature of Inventor 207:			Date:	
2	Full Name Of Inventor	Family Name MARRINGA	First Given Name Menno	Second Given Name
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship Netherlands
8	Post Office Address	Post Office Address 25 Conrad Street	City San Francisco	State & Zip Code/Country California 94131 U.S.A.
Signature of Inventor 208:			Date:	
2	Full Name Of Inventor 9-00	Family Name DUKATZ	First Given Name Eric	Second Given Name S.
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Signature of Inventor 209: X <i>Wm Dm</i>			Date: X 4/18/01	

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

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(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

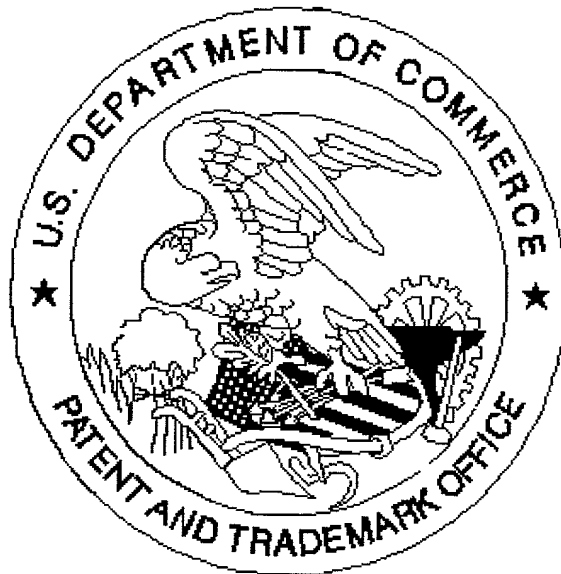
(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

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